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MS-7543 ATX Version: 0C

CPU: BloomField Processors In LGA1366 Package.

System Chipset:

Intel Tylersburg I/O Hub 36S (North Bridge)
Intel ICH10R (South Bridge)

On Board Devices:

CLOCK Gen -- ICS 9LPRS113
LPC Super I/O -- Fintek F71882F
Dual LAN --BCM5784M
HD Audio Codec -- ALC888S
1394 Controller -- TI TSB43AB22A
ODD_SATA /IDE -- JMB363
eSATA -- SIL3123

Main Memory:


3-Channel A / B / C DDR-III *3

Expansion Slots:

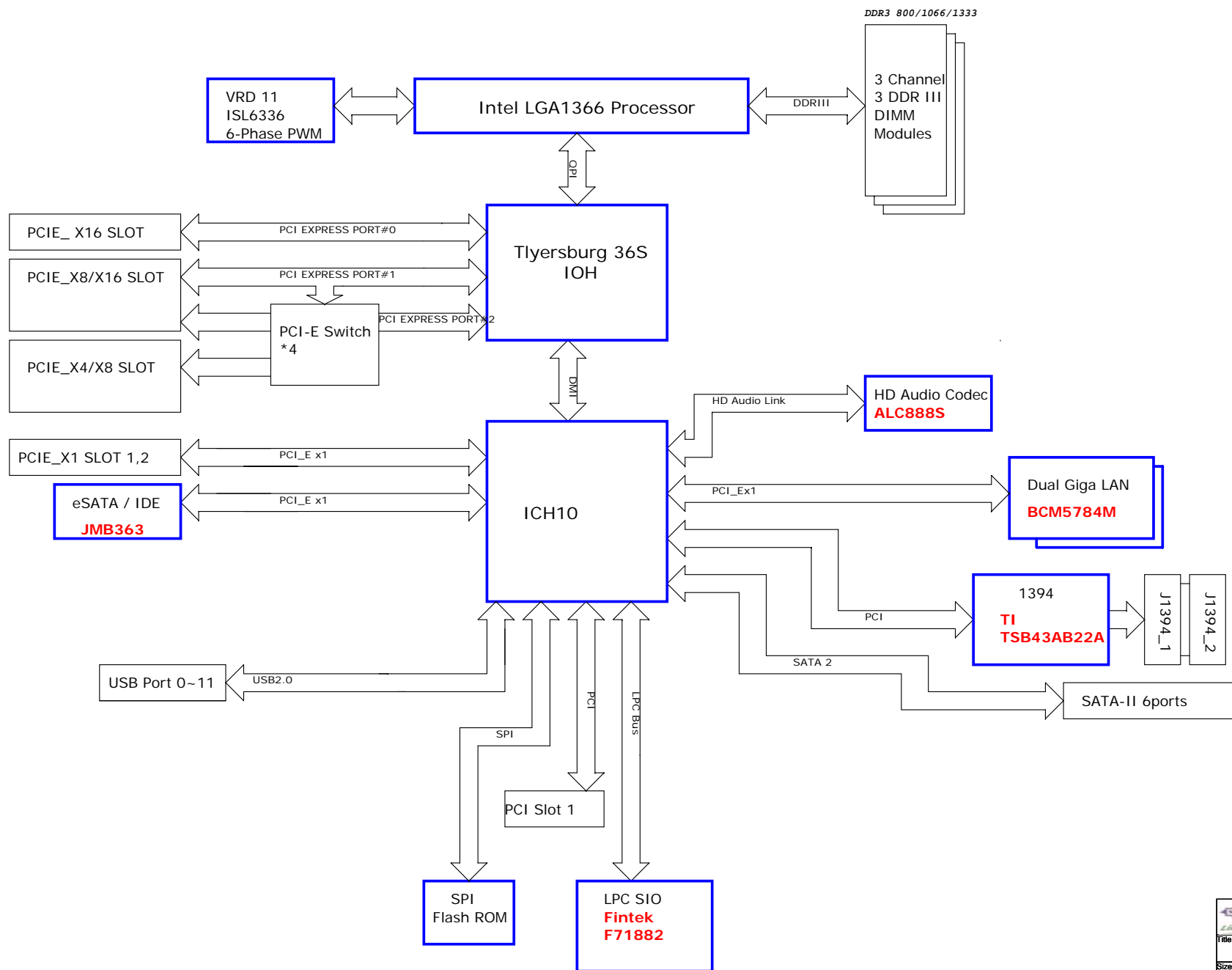
PCI EXPRESS X16 SLOT *3
PCI EXPRESS X1 SLOT * 2
PCI SLOT * 1

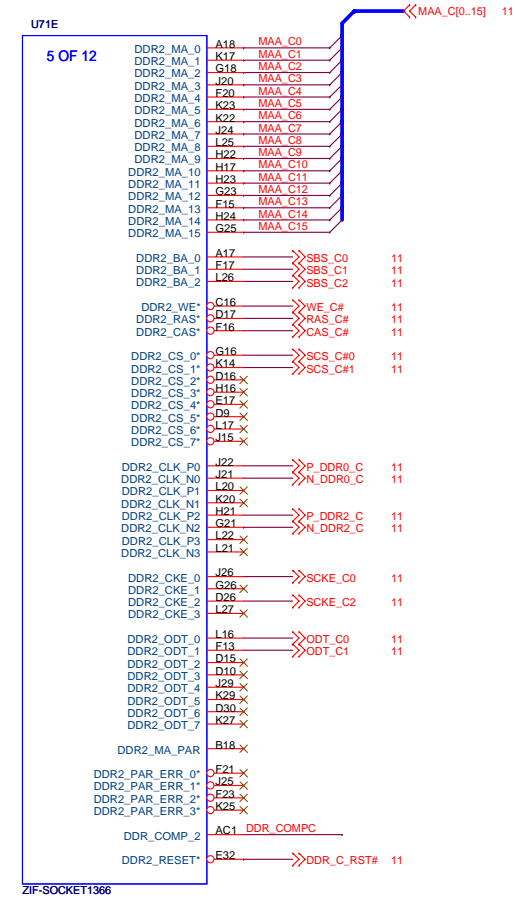
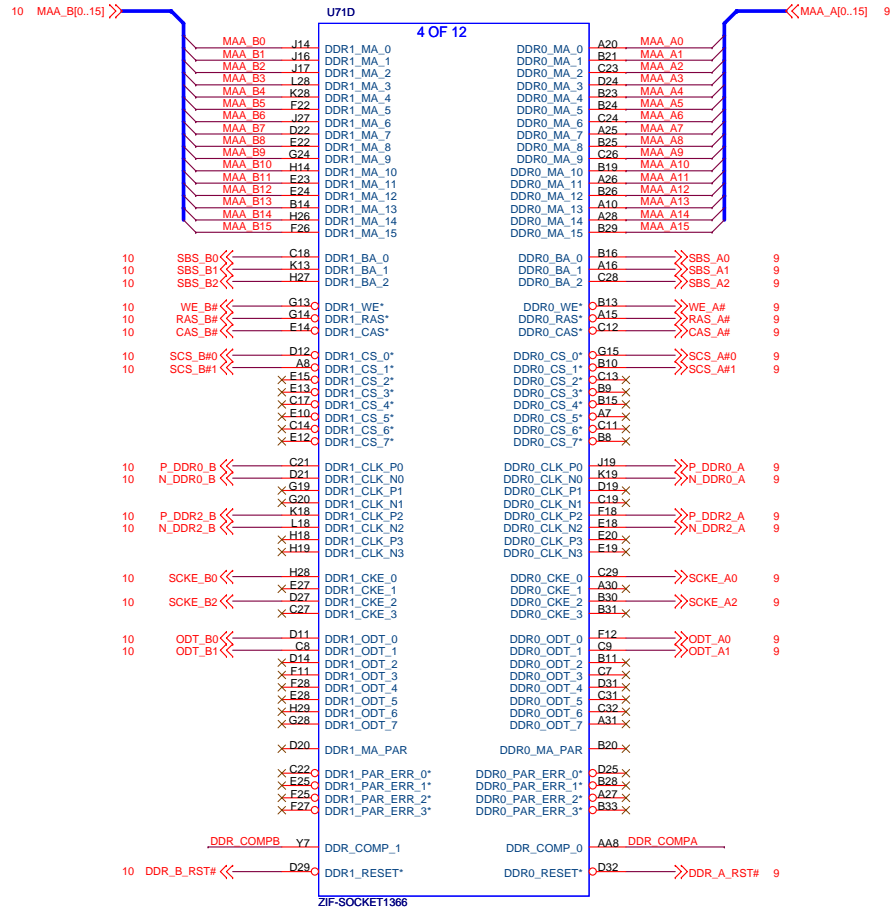
PWM: VR11.1 Intersil ISL6336 (6 Phases)

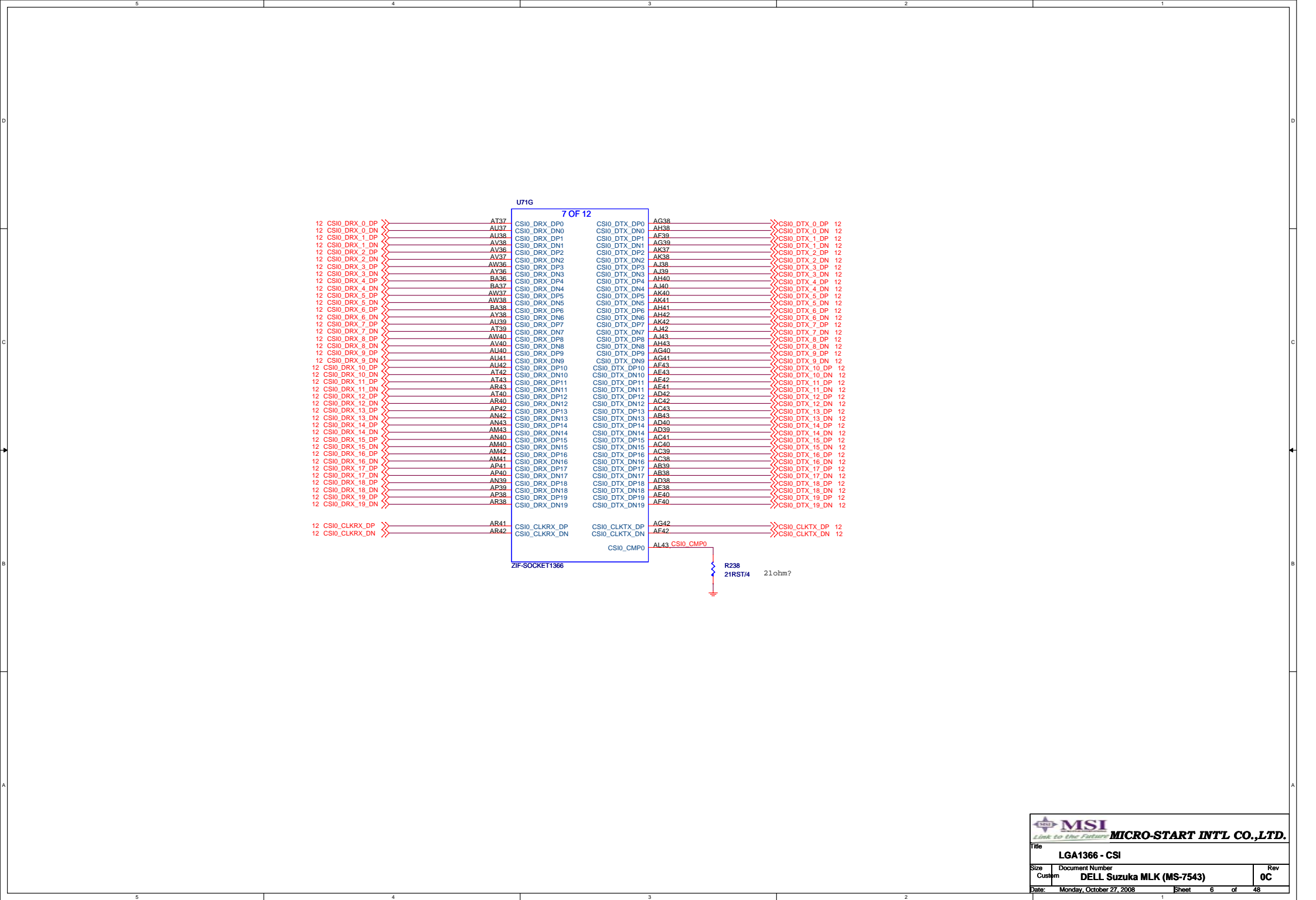
DELL Suzuka MLK

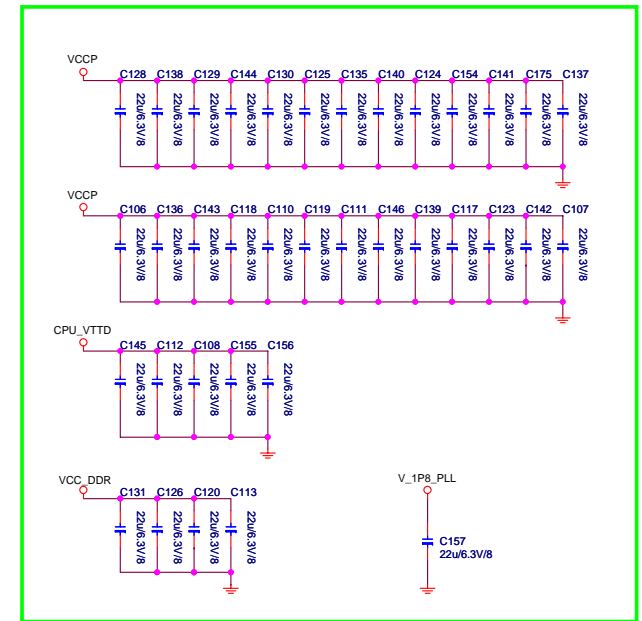
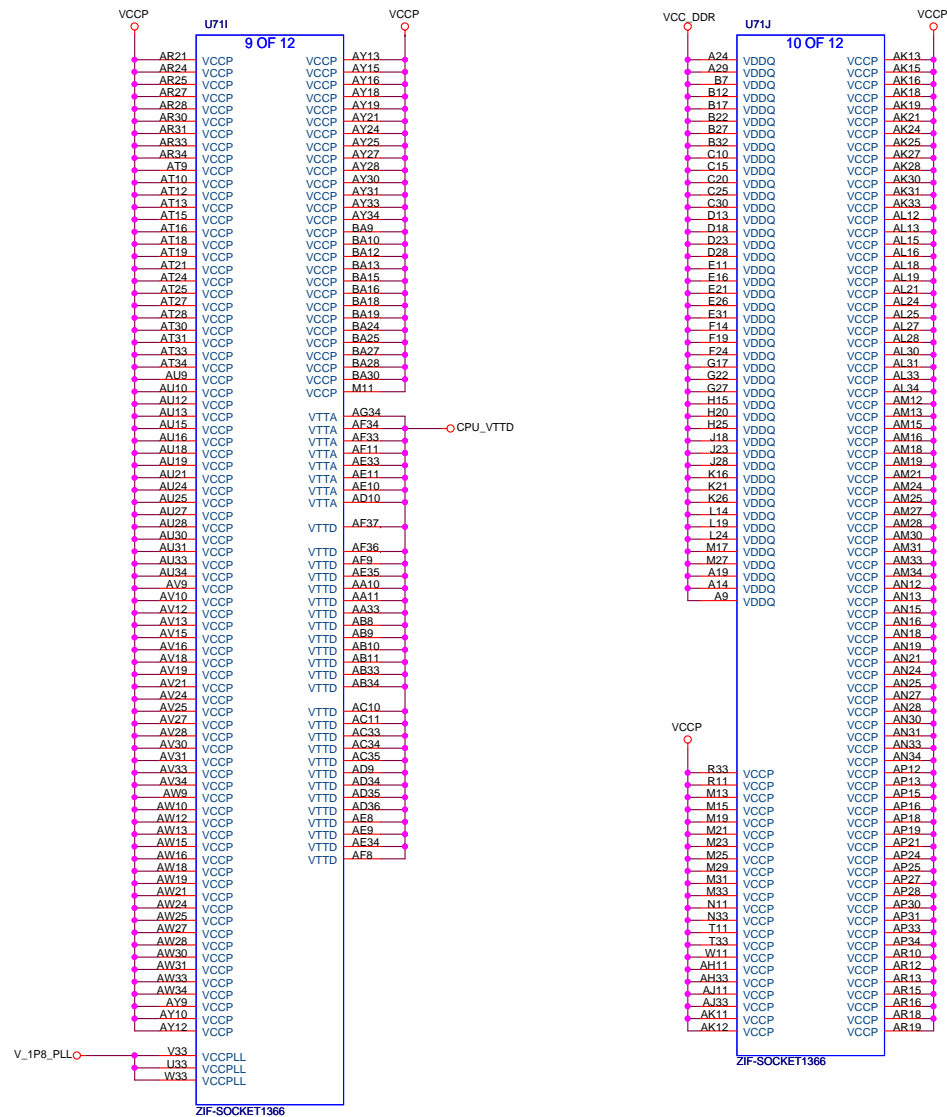
 MICRO-START INT'L CO.,LTD.		
Title COVER SHEET		
Size	Document Number	Rev
Custom	DELL Suzuka MLK (MS-7543)	0C
Date:	Monday, October 27, 2008	Sheet 1 of 48

Block Diagram

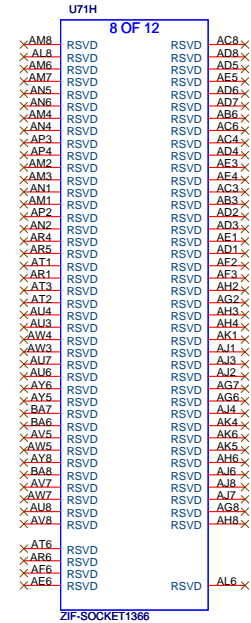
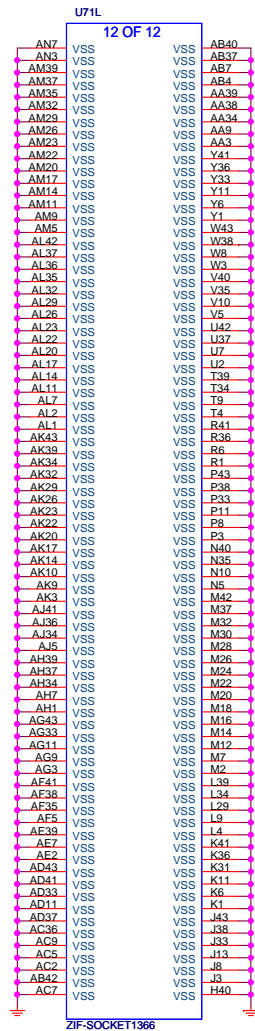
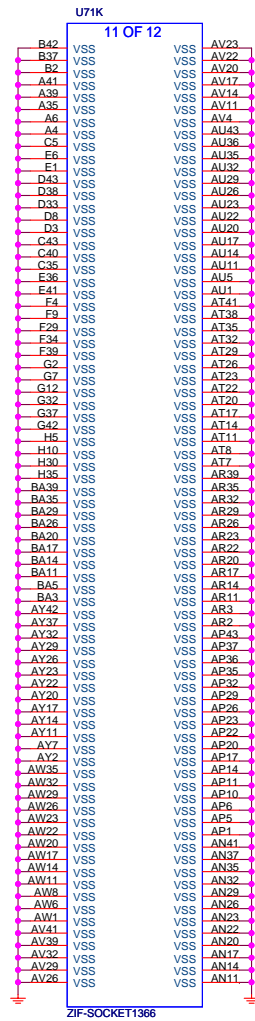




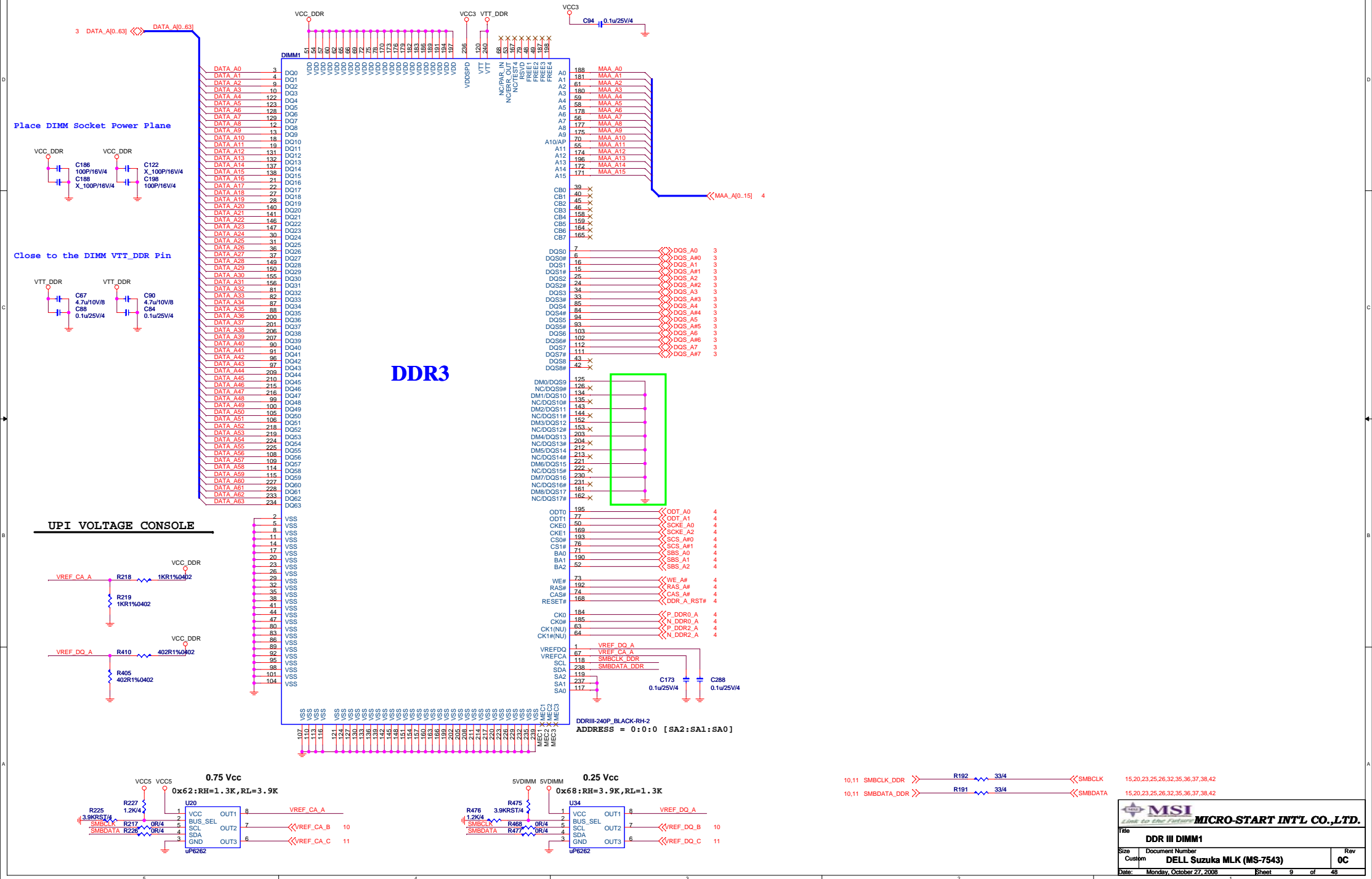




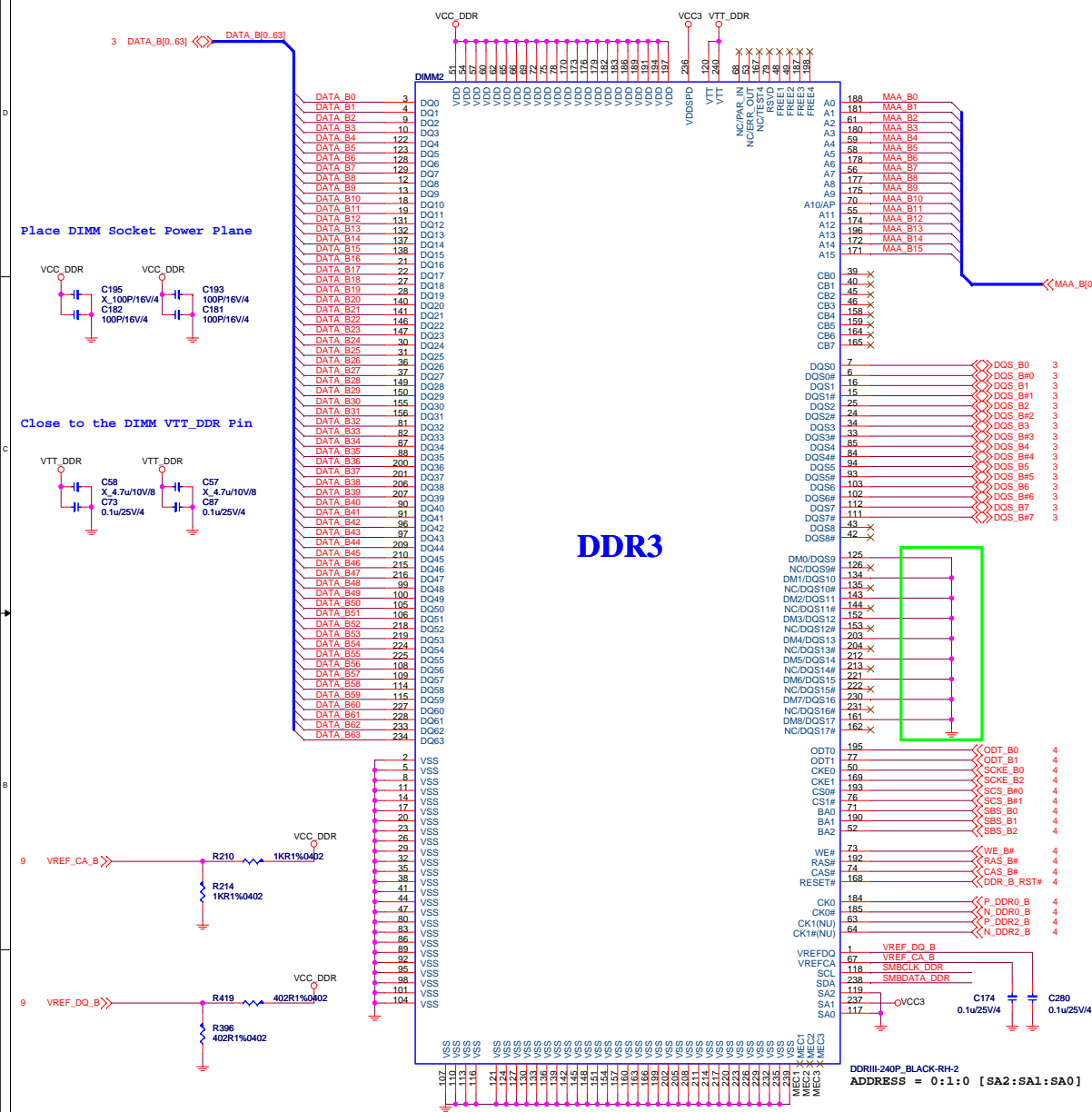
INSIDE CPU SOCKET



DIMM1 / CHANNEL A0



DIMM2 / CHANNEL B0



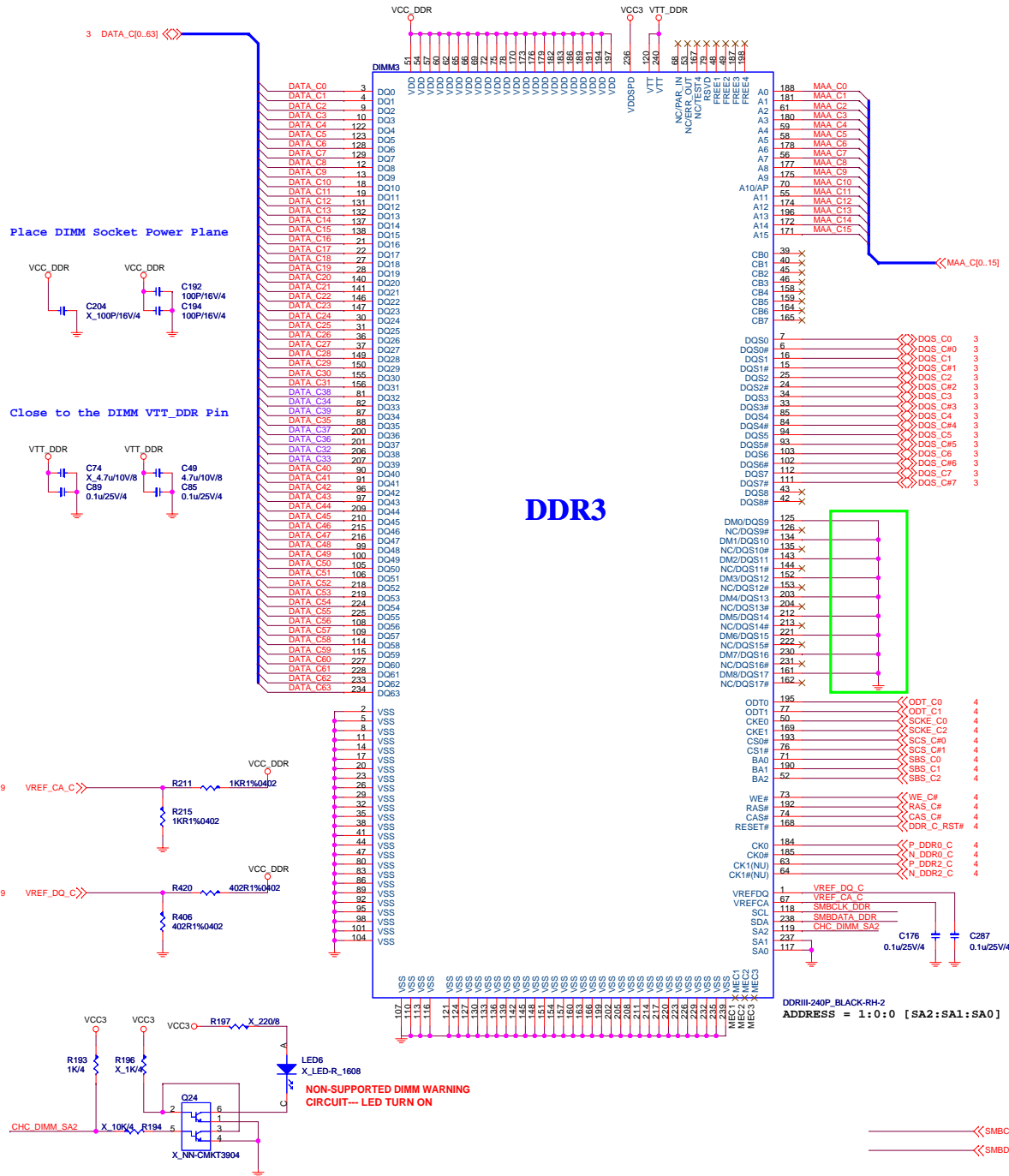
Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

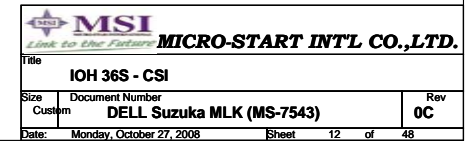
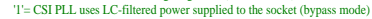
Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

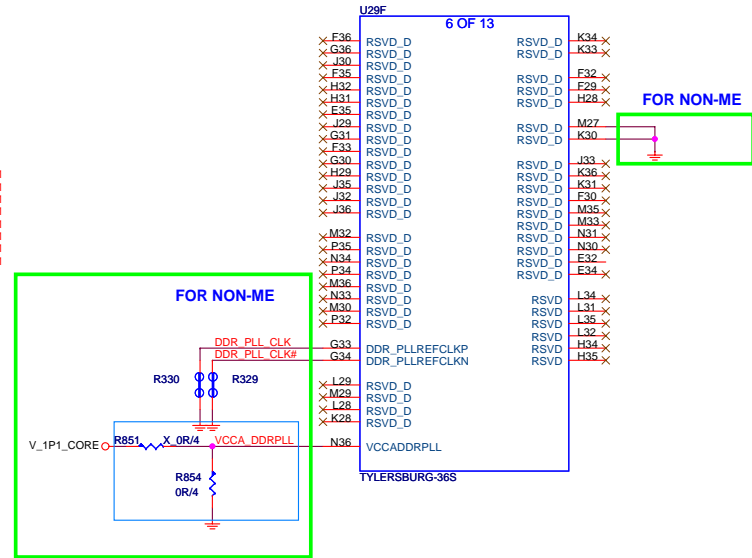
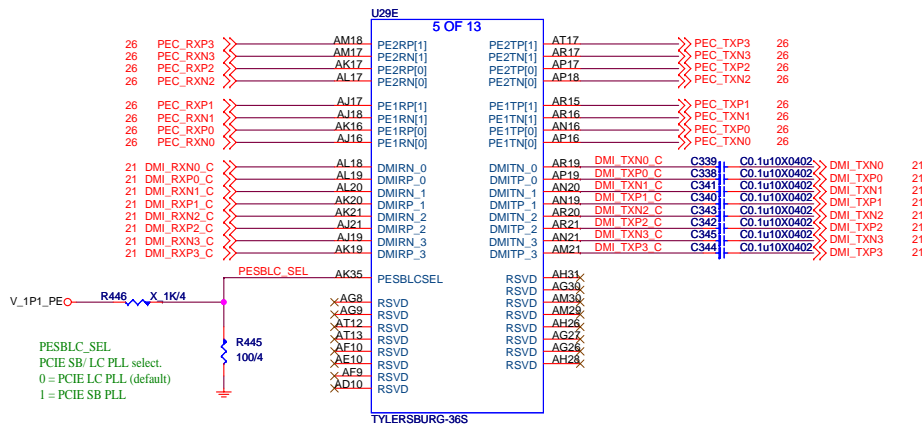
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

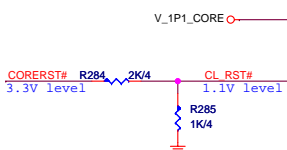
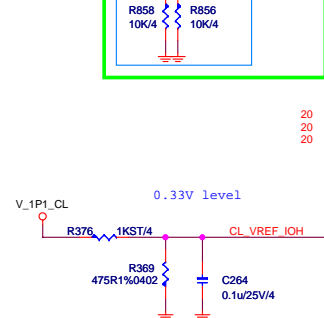
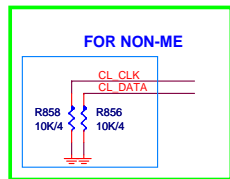
 SMBCLK_DDR 9,11
 SMBDATA_DDR 9,11

DIMM3 / CHANNEL C0









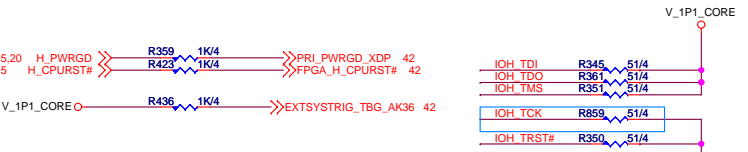
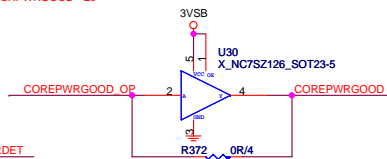
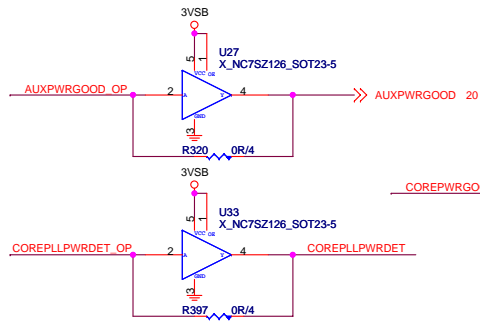
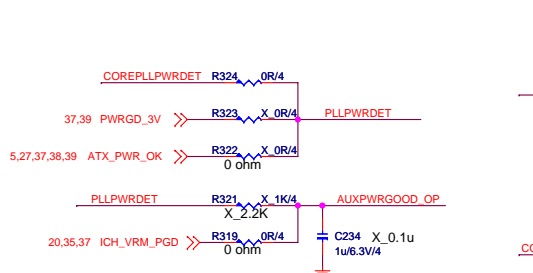
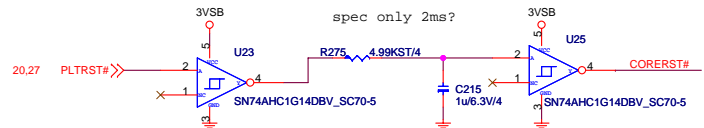
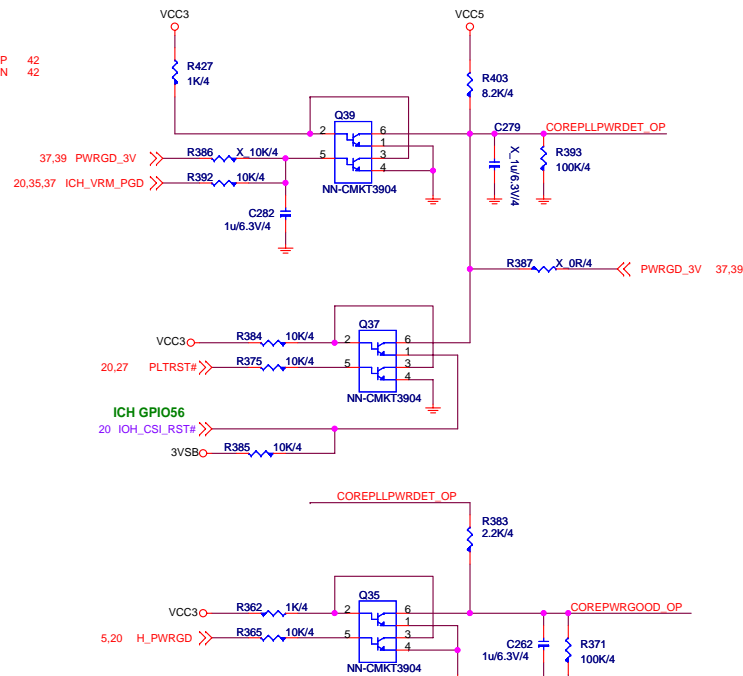
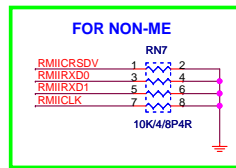
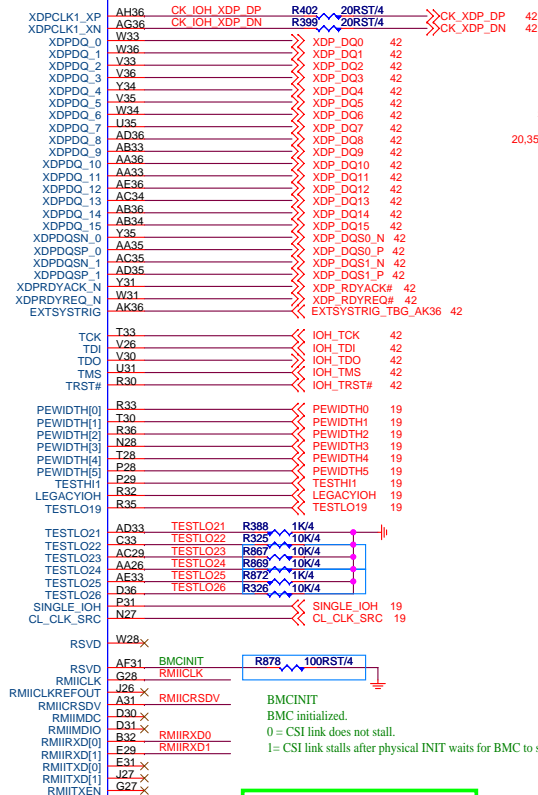
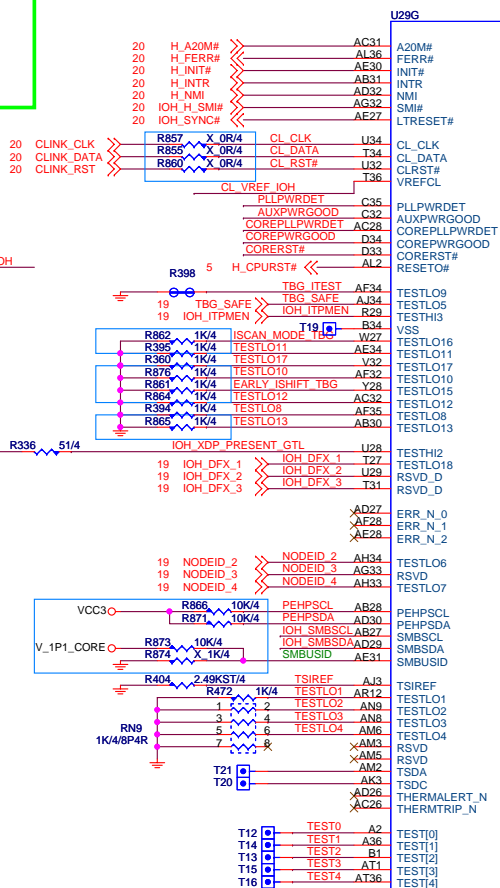
SMBUSID

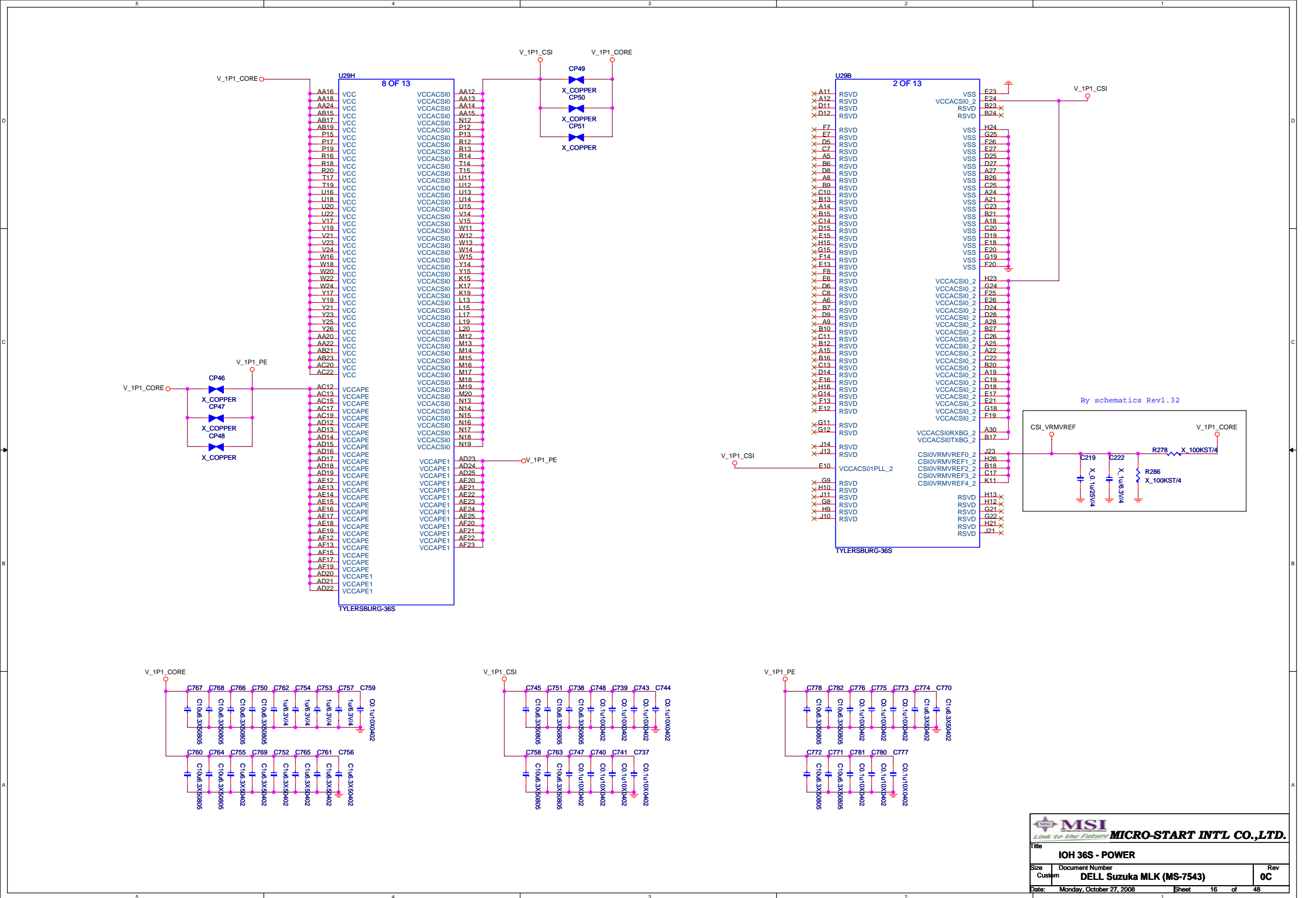
SMBus ID: Indicates SMBus ID bits [7:4].

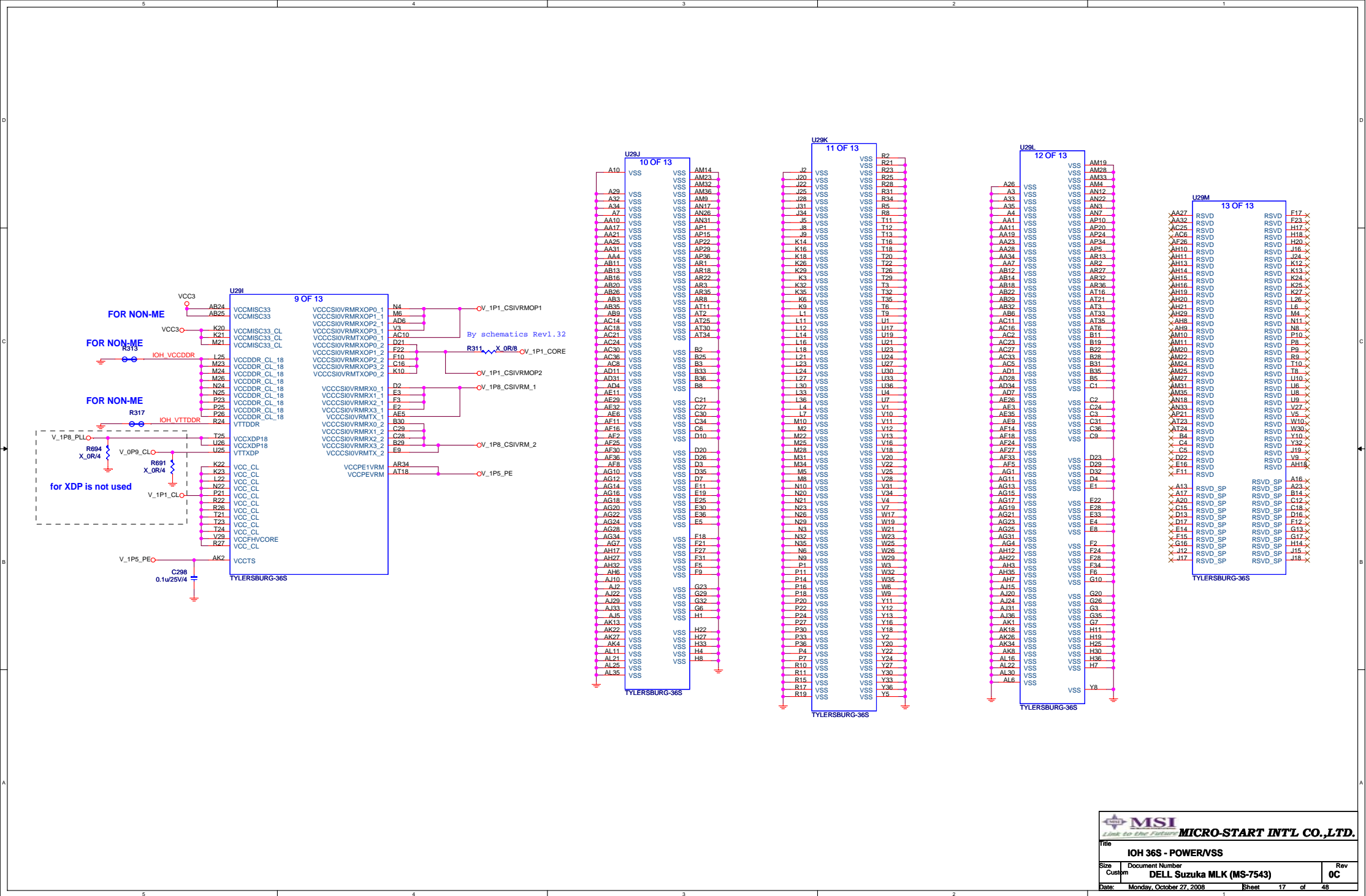
'1' indicates an upper-address ID of 1110 (0xE).

'0' indicates an upper-address ID of 1100 (0xC).

IOH SMBUSCL/SMBSDA/SMBUSID not support yet





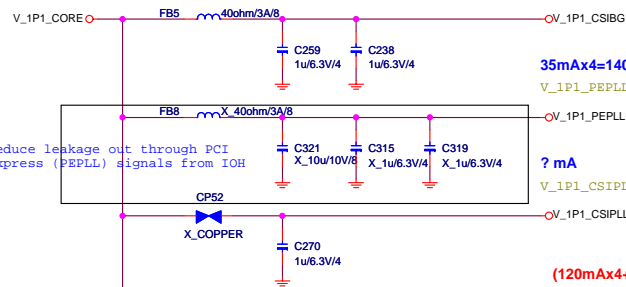


V_1P1_CORE REPLACE WITH V_1P1_VCCA

0.7A???

10mA \times 2=20mA

V_1P1_CSIBG = CSIBG_RX+CSIBG_TX



35mA \times 4=140mA

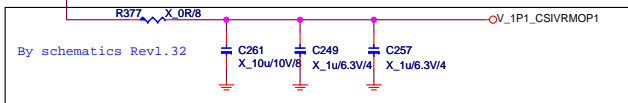
V_1P1_PEPLL = PEPLLA+PEPLLD

? mA

V_1P1_CSIPLL = CSI_PLL

(120mA \times 4+60mA)??=0.54A ?????

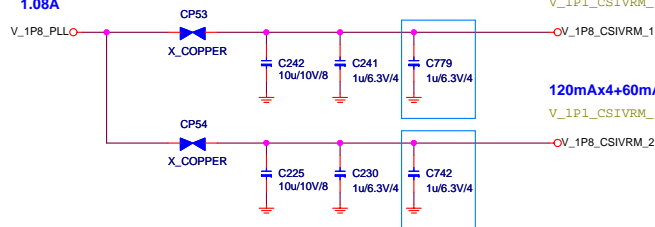
V_1P1_CSIVRMOP1 = CSIVRMOP_RX[1:4]+CSIVRMOP_TX1



1.08A

120mA \times 4+60mA=0.54A

V_1P1_CSIVRM_1 = CSIVRM_RX_1+CSIVRM1_TX_1



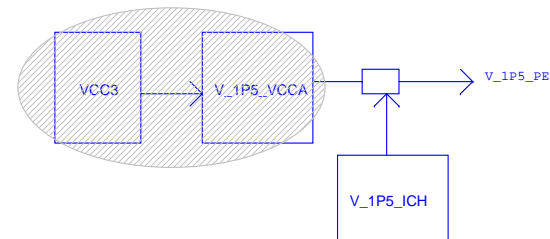
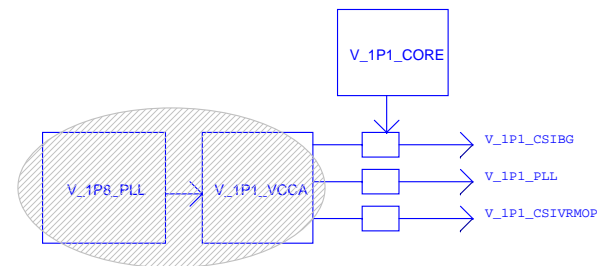
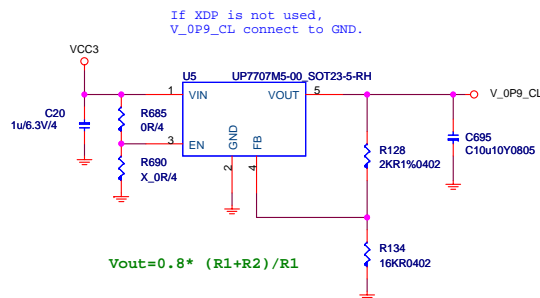
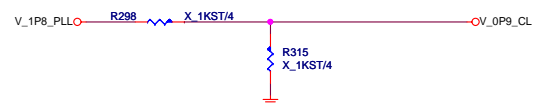
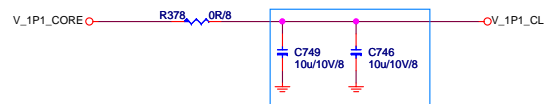
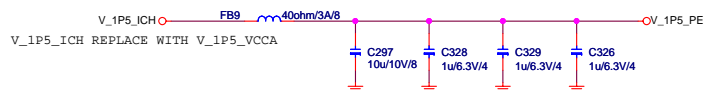
120mA \times 4+60mA=0.54A

V_1P1_CSIVRM_2 = CSIVRM_RX_2+CSIVRM1_TX_2

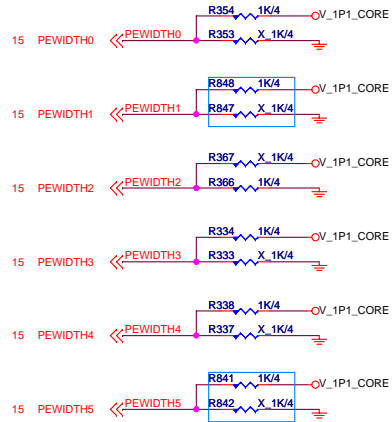
186.3mA+?

92mA \times 2+1.15mA \times 2+=186.3mA+?

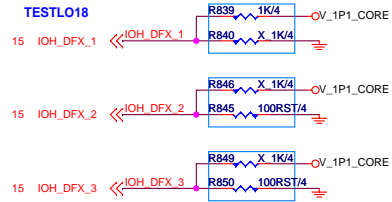
V_1P5_PE = PEVRM+PEBG0+PEBG1+VCCTS



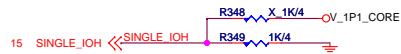
PEWIDTH0-5
PCIE Link Width Select
"111011" = 2x16
"101111" = 4x8
"011111" = Wait On Bios



IOH_DFX_2, 3}
DDR frequency selection pins:
DDRFRFREQ[3:2] as DDR frequency selection defined as:
"00" = 133MHz input, 200MHz core
"01" = 100 MHz input, 200MHz core
"10" = RSVD
"11" = RSVD



SINGLE_IOH
Used for dual TBG IOH selection:
"0": IOH is not connected to another IOH on some CSI link (default)
"1": IOH is connected to another IOH on some CSI link



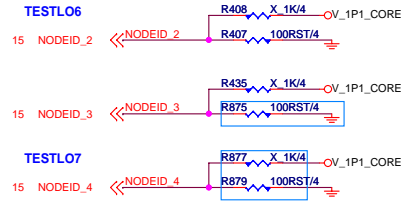
CL_CLK_SRC
Used for ME default clock source:
"1": PLL (default) -- EXT ME CLK
"0": Ring Oscillator (back-up) -- INT ME CLK



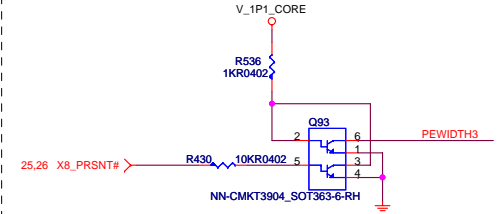
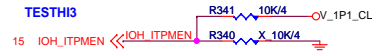
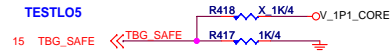
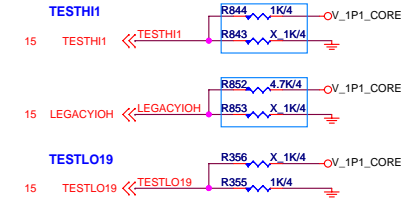
NON-ME FUNCTION

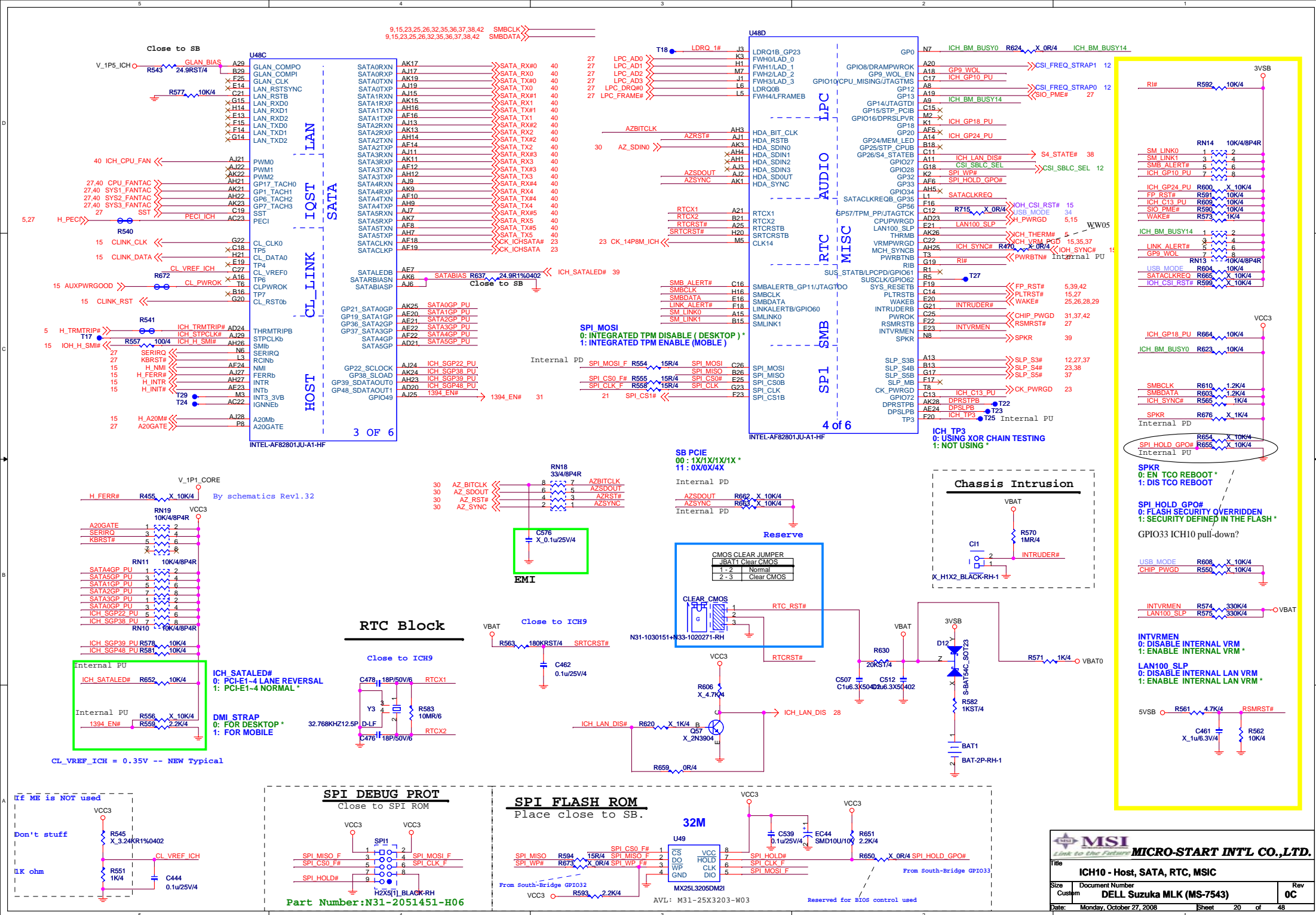
VCCADDRPLL and ME_CLK_SRC
pins must be tied to VSS as well

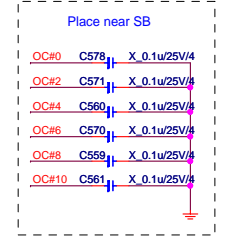
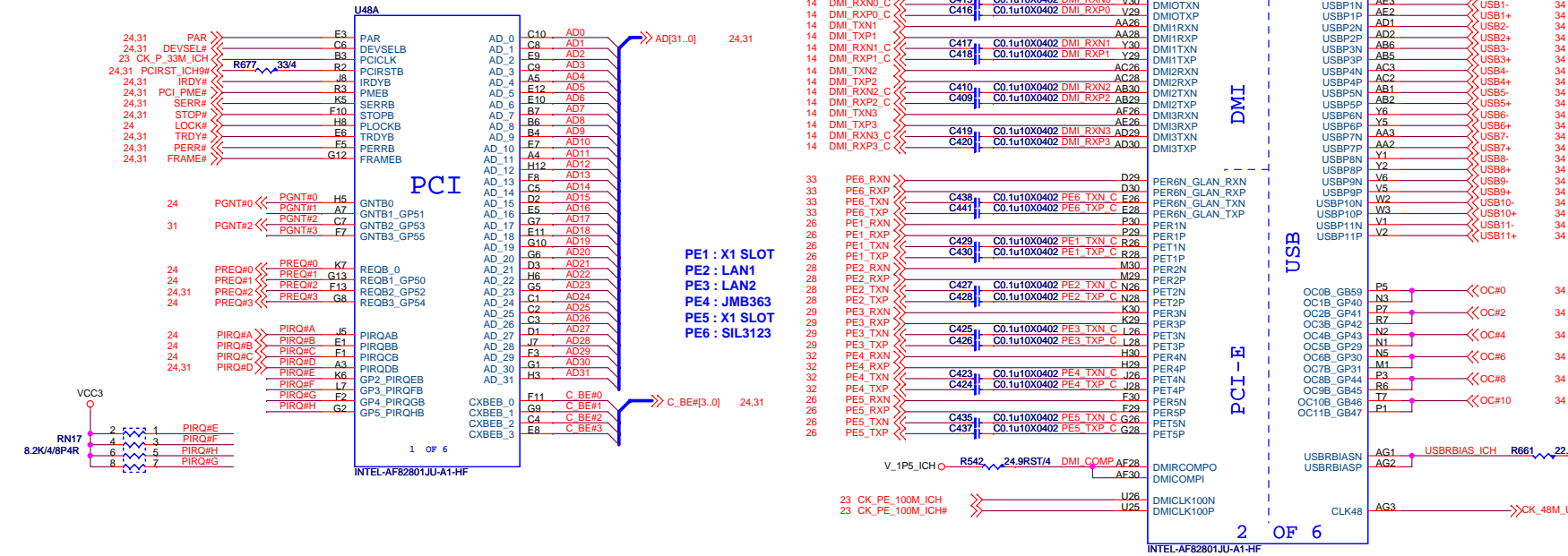
NODEID_3_TBG
For dual TBG IOH configuration,
it indicates which CSI port is connected to the other IOH.
"0": CSI0
"1": CSI1



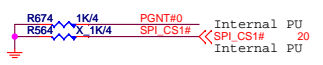
LEGACYIOH
Used to determine legacy or non-legacy selection:
"1": Legacy IOH
"0": Non-legacy IOH



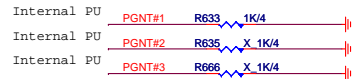




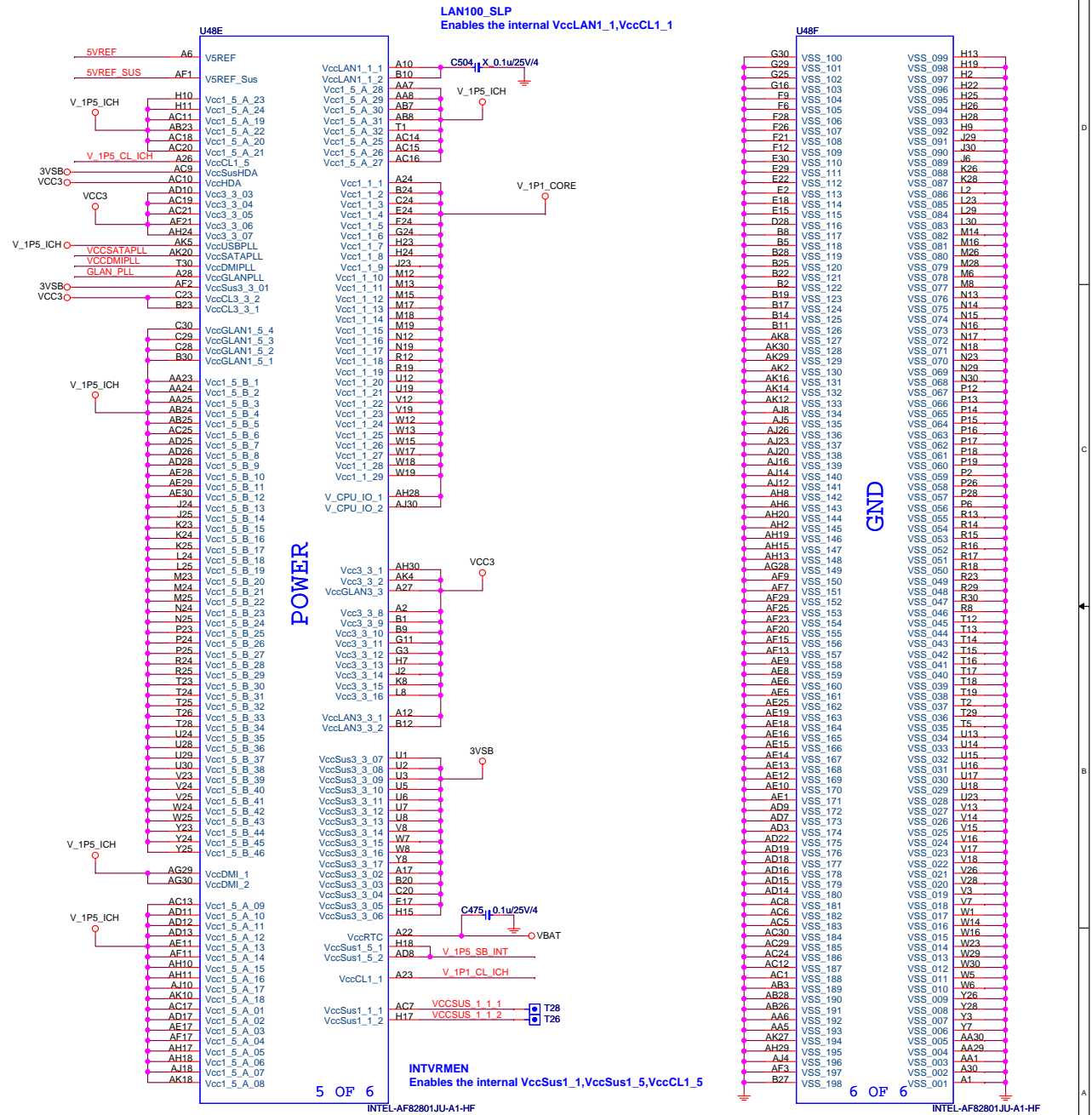
SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
LPC	1	1
SPI	0	1
PCI	1	0



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)
GNT1	DC	AC	DMI AC/DC MODE 0 : AC 1 : DC

[illegible]

0: Pin21/22 100MHz*
1: Pin21/22 96MHz

GSEL_33M_CLK **R643** **X 4.7K/4**

Internal pull down

0: PCICLK4
1: RESET*

_WDT#_R **R642** **4.7K/4**

Internal pull down

0: PCIE9*
1: CPU_1TP

1TP_EN **R605** **X 4.7K/4**

Internal pull down

1: 25MHz freerun function

CK_25M_0F **R641** **X 4.7K/4**

R646 **X 4.7K/4**

Internal pull up

1 = Selects pin 29/30 to be PCI_STOP#/CPU_STOP#

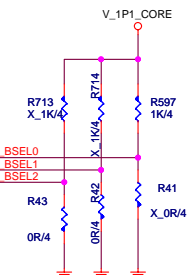
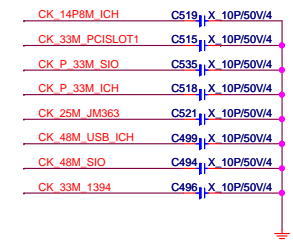
CK_25M_1 **R647** **X 4.7K/4**

Internal pull down

For ICS CPU/DIV SEL
0: FSLD BIT3 = 0*
1: FSLD BIT3 = 1

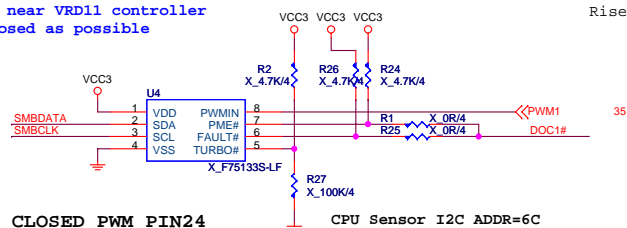
FSD_33M_CLK **R631** **4.7K/4**

Internal pull up



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz
0	0	1	133 MHz (default)
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	333 MHz
1	0	1	100 MHz
1	1	0	400 MHz
1	1	1	200 MHz

Place near VRD11 controller
as closed as possible



```
Vimon= (Riout / N) x (Rx/Risen) x Iload
Riout = Rimon
Rx = DCR
Risen = ISEN+
```

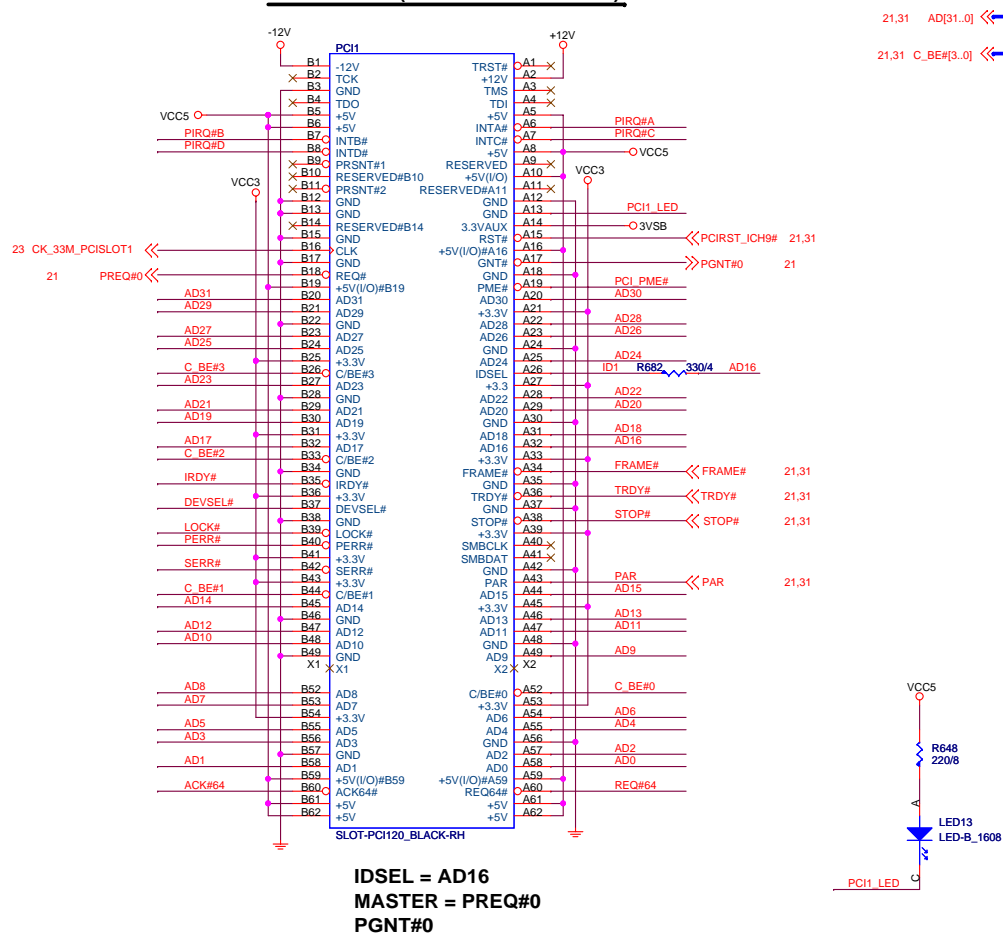
DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

 **MSI**
Link to the Future **MICRO-START INT'L CO., LTD.**

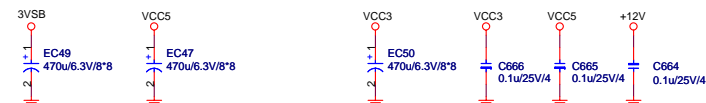
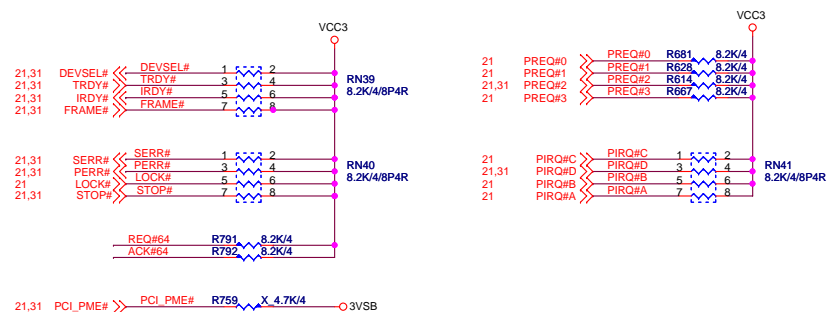
Title	Clock Gen ICS9LPRS113
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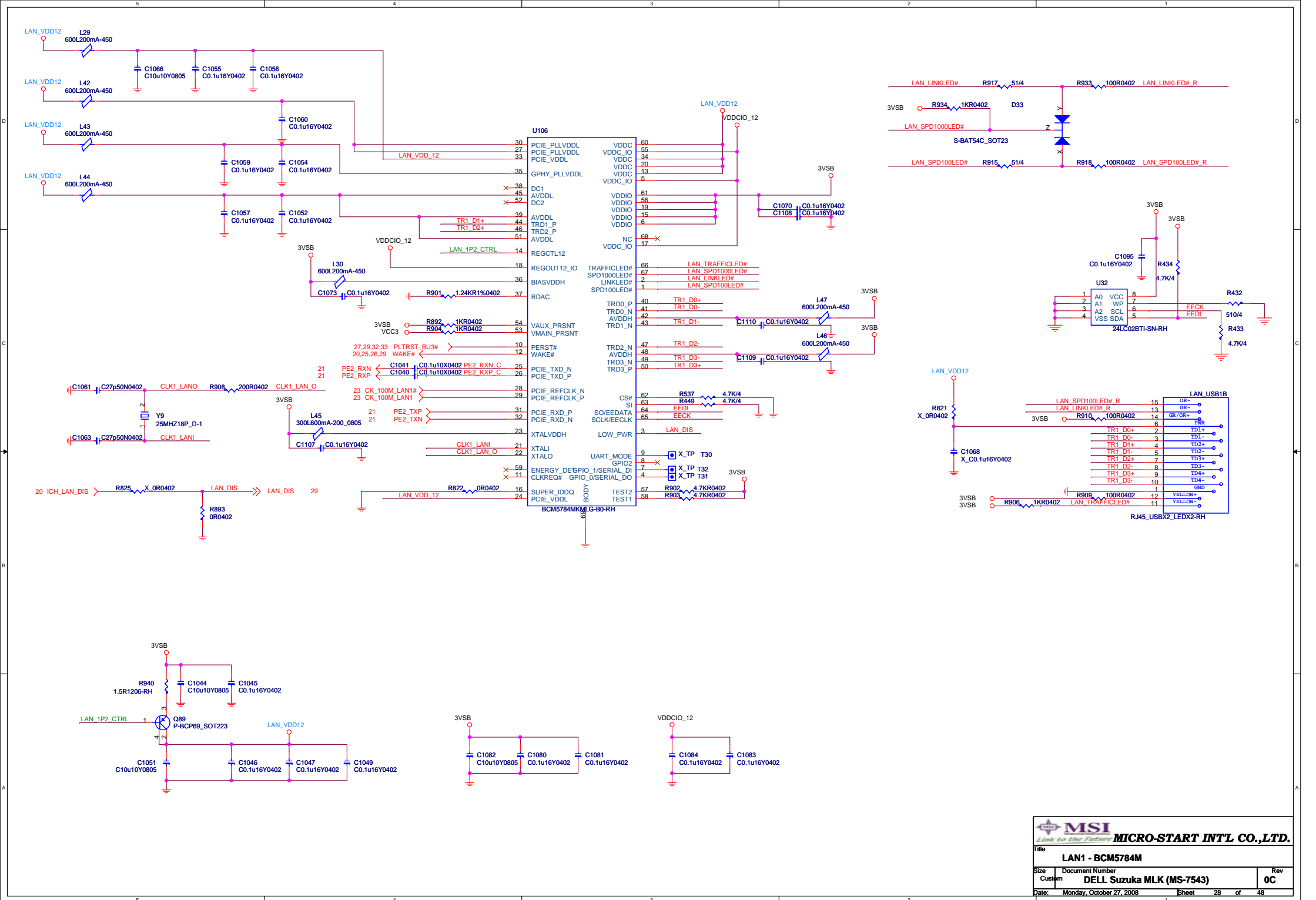
Size	Document Number	Rev
Custom	DELL Suzuka MLK (MS-7543)	0C

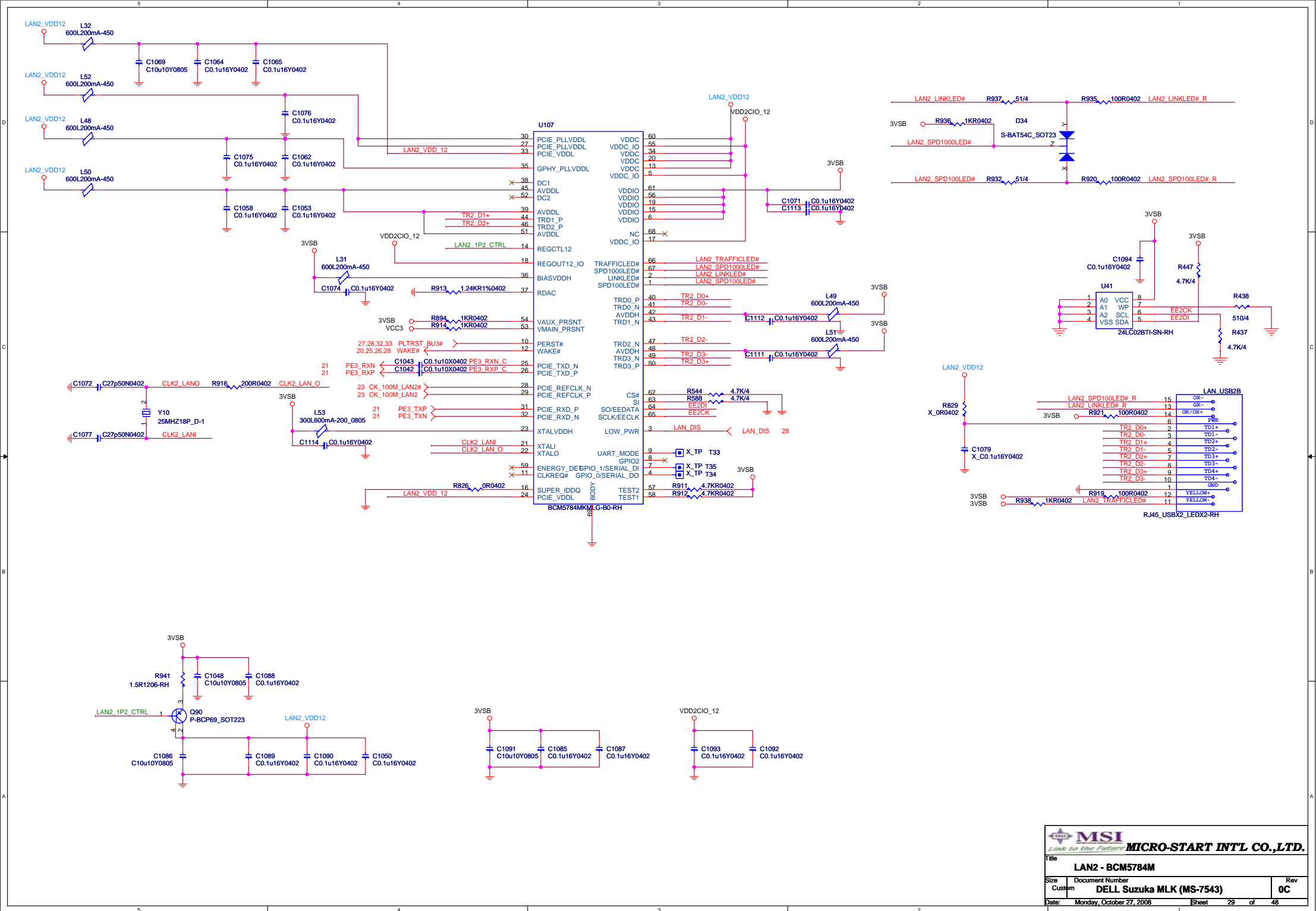
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

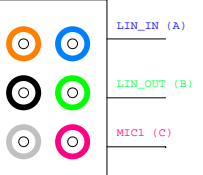
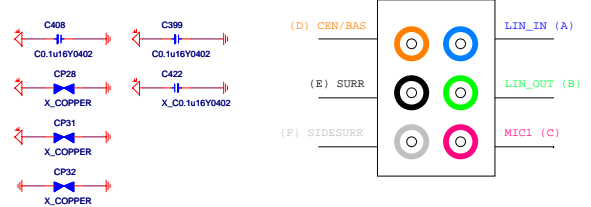
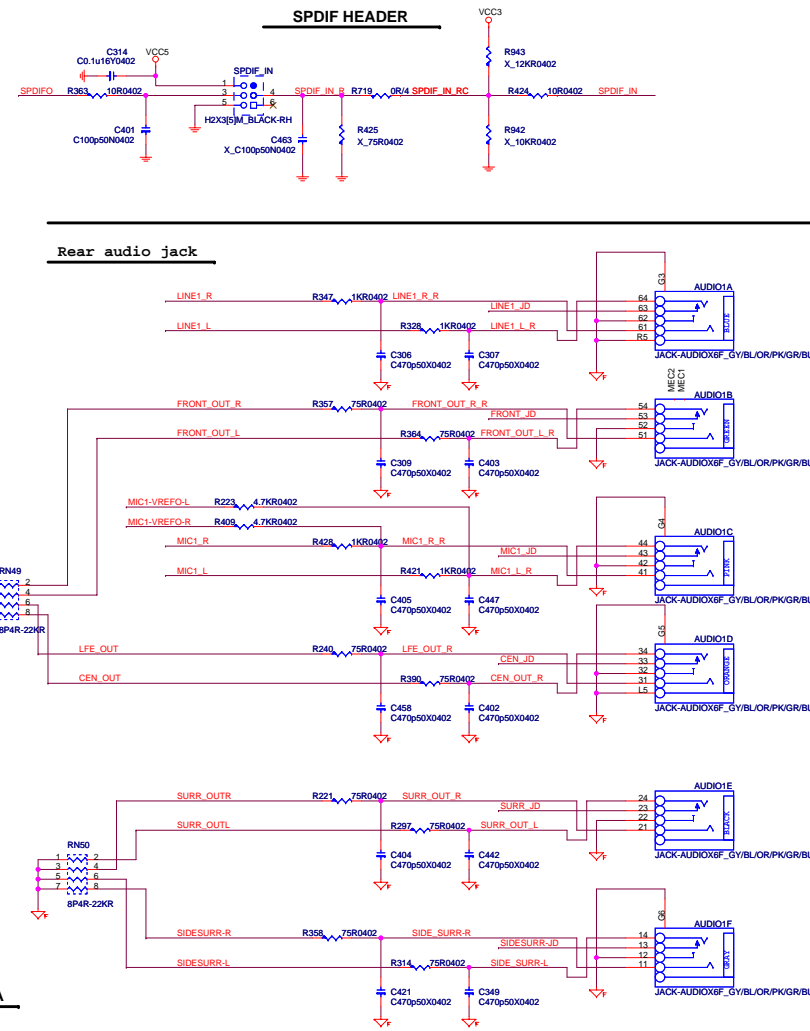
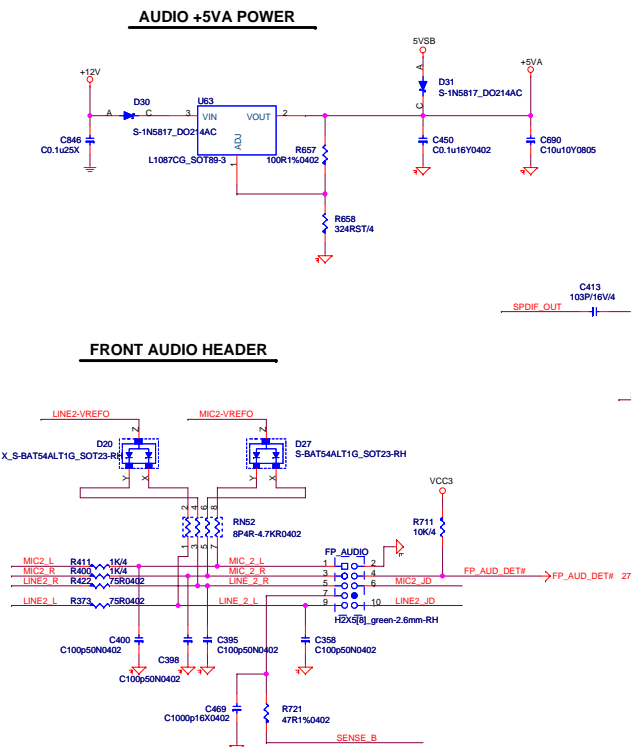
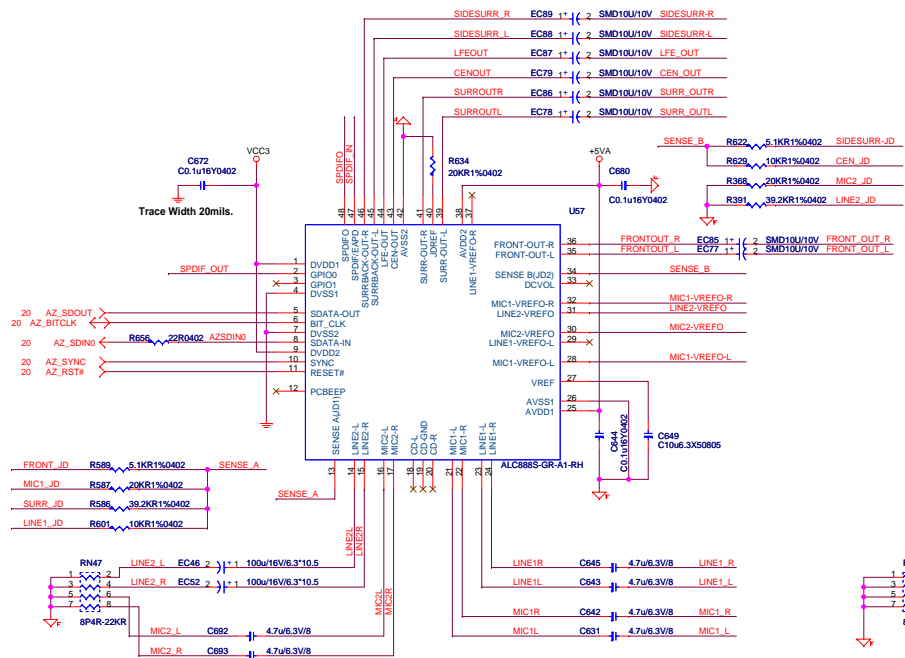


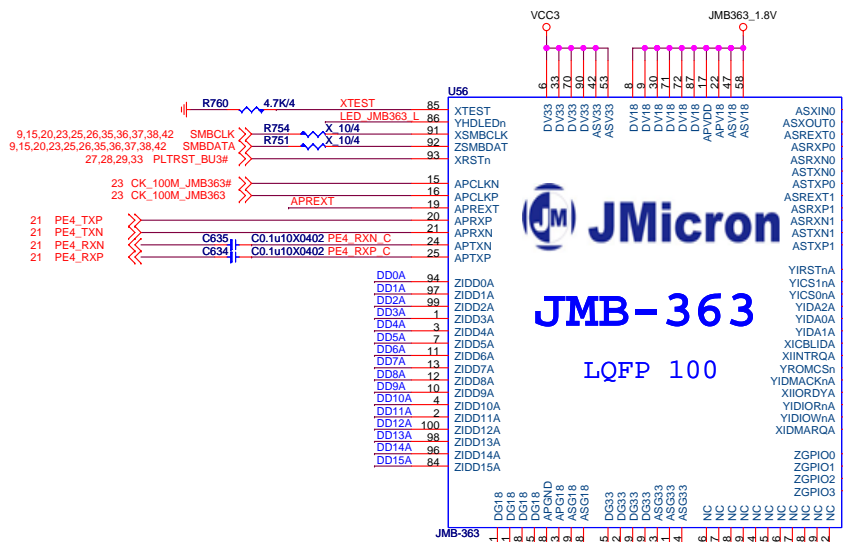
PCI PULL-UP / DOWN RESISTORS



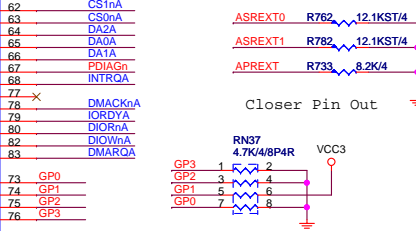
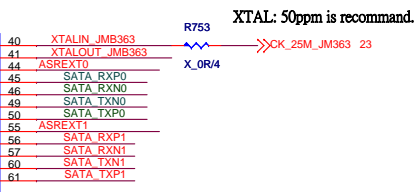




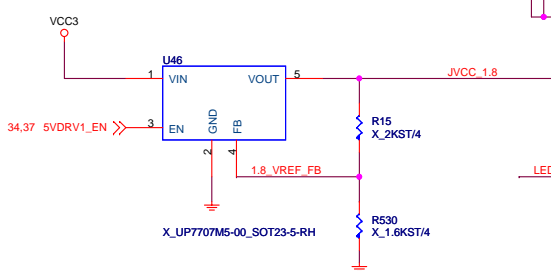
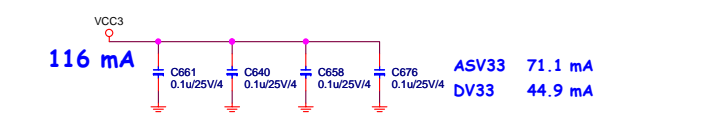
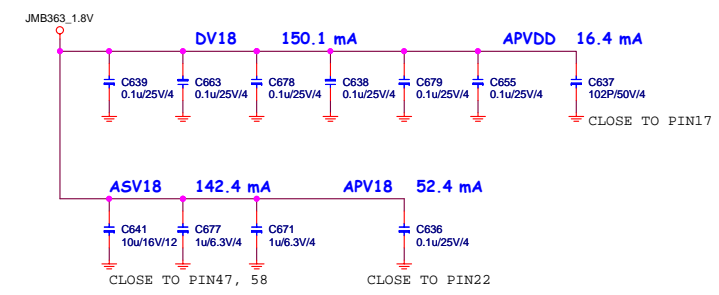
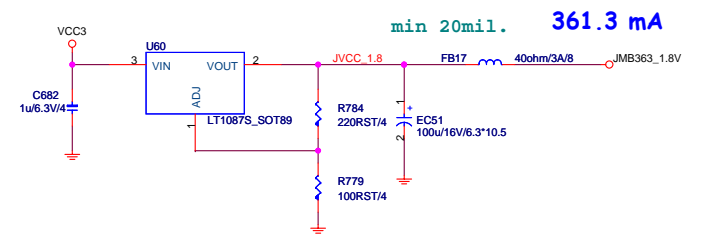
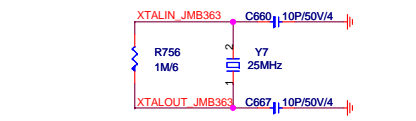




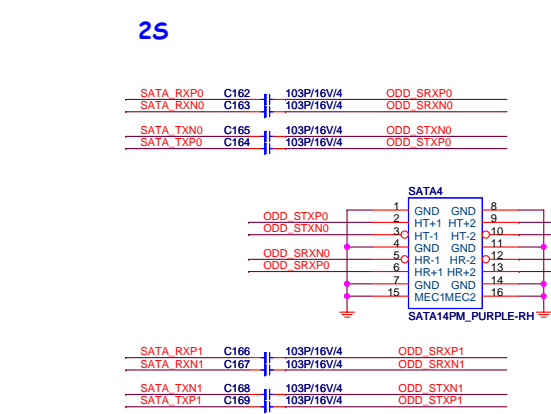
JMicron JMB-363 LQFP 100



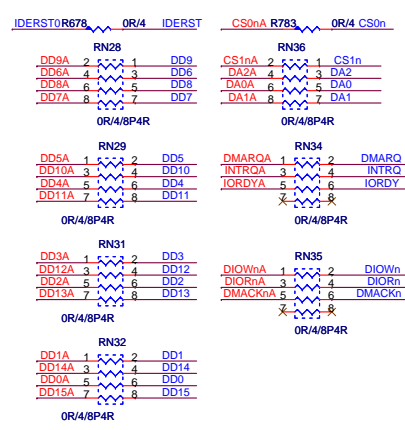
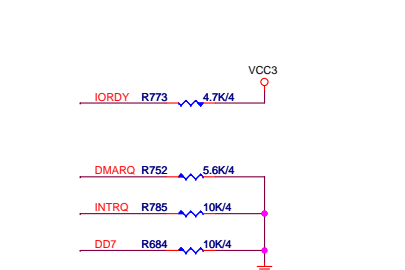
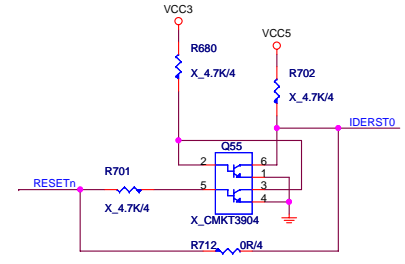
GPIO1 is clock source
 0: from internal clock source
 1: from ASXIN & ASXOUT



UP7707
 $V_{OUT} = 0.8 \times (R1 + R2) / R1$

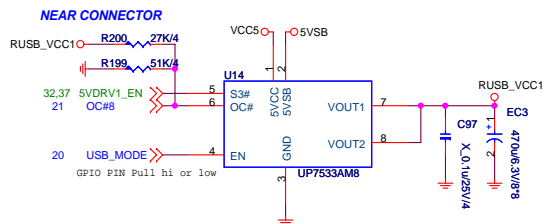


1P

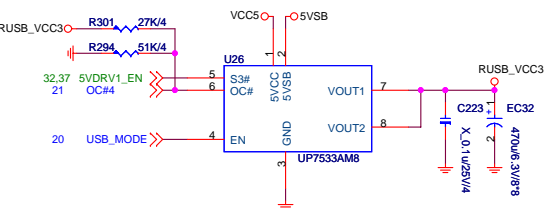


if the length of JMB-363 to IDE connector more than 4inch, that must stuff damping resistor.

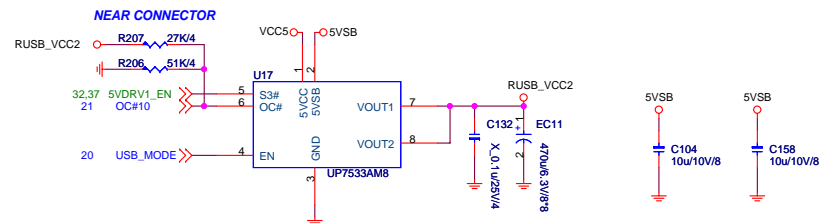
USB POWER FOR PORT 0,1



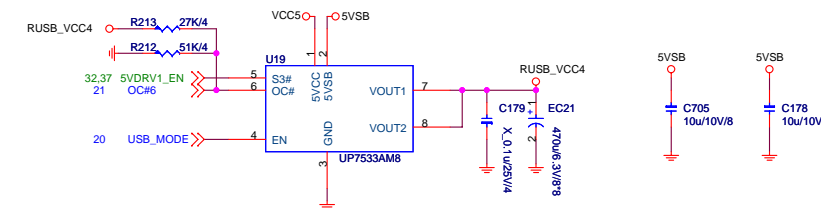
USB POWER FOR PORT 4, 5



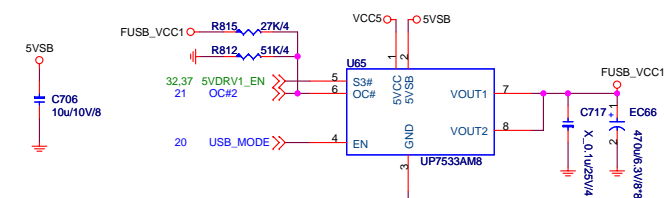
USB POWER FOR PORT 2,3



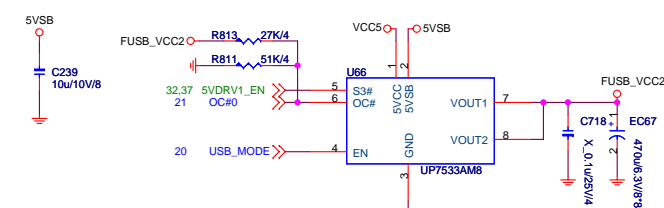
USB POWER FOR PORT 6,7



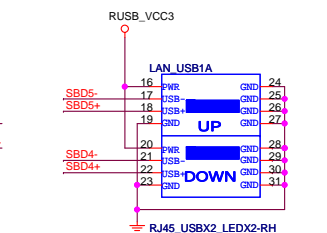
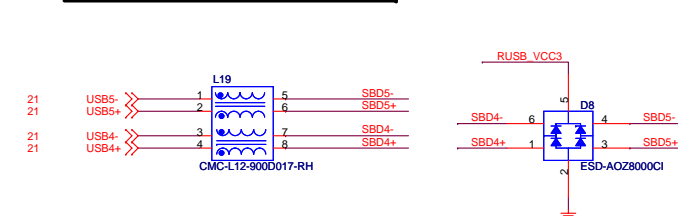
USB POWER FOR PORT 8,9



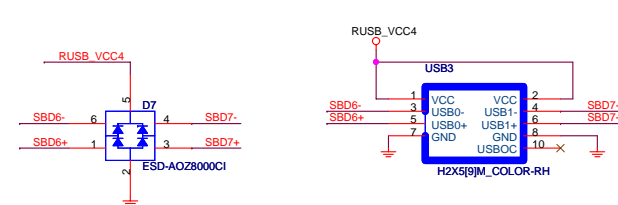
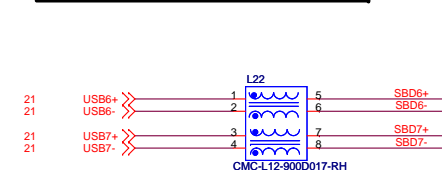
USB POWER FOR PORT 10,11



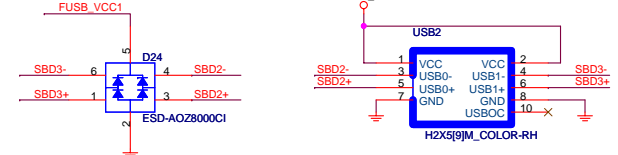
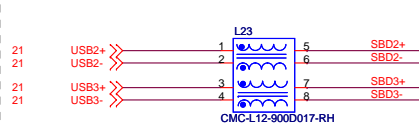
REAR USB PORT 4,5 (With LAN)



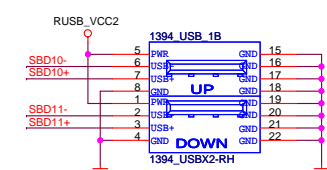
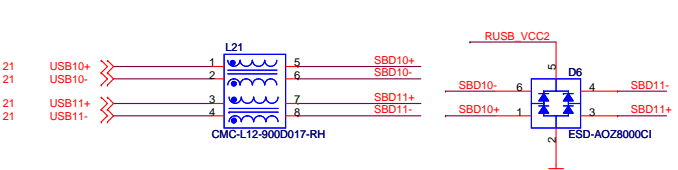
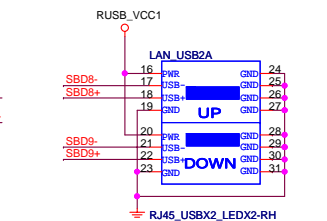
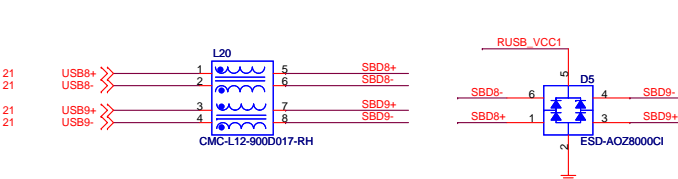
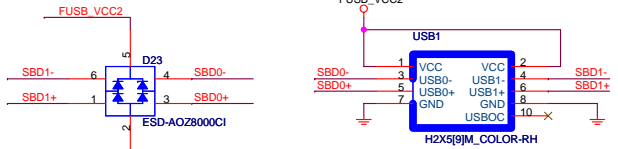
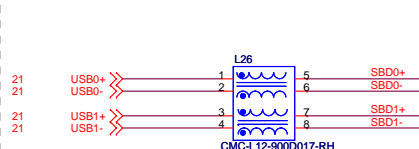
REAR USB PORT 6,7 (With LAN)



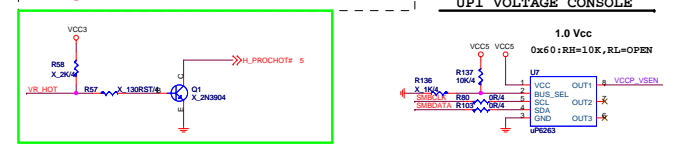
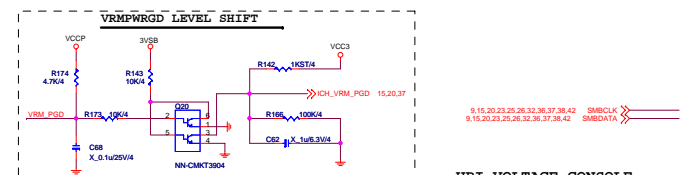
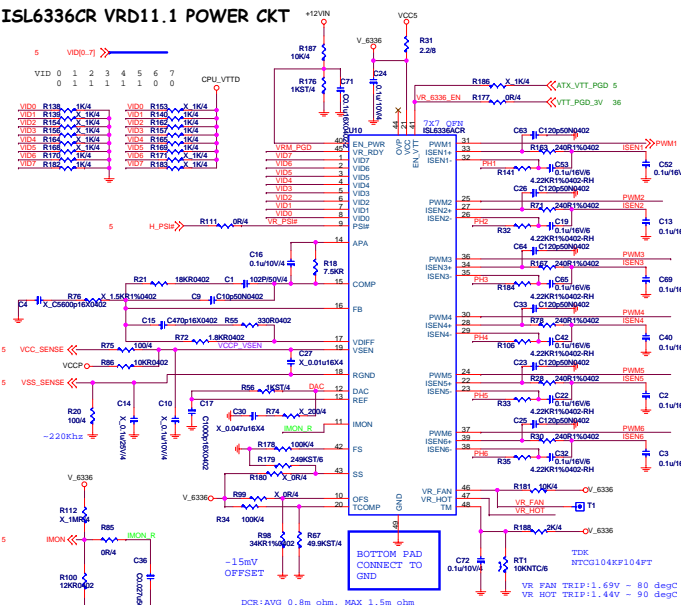
FRONT USB PORT 8,9



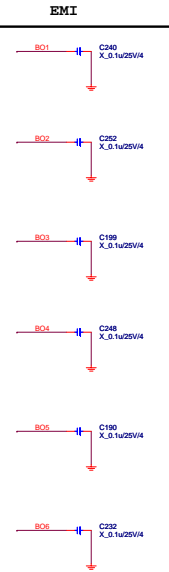
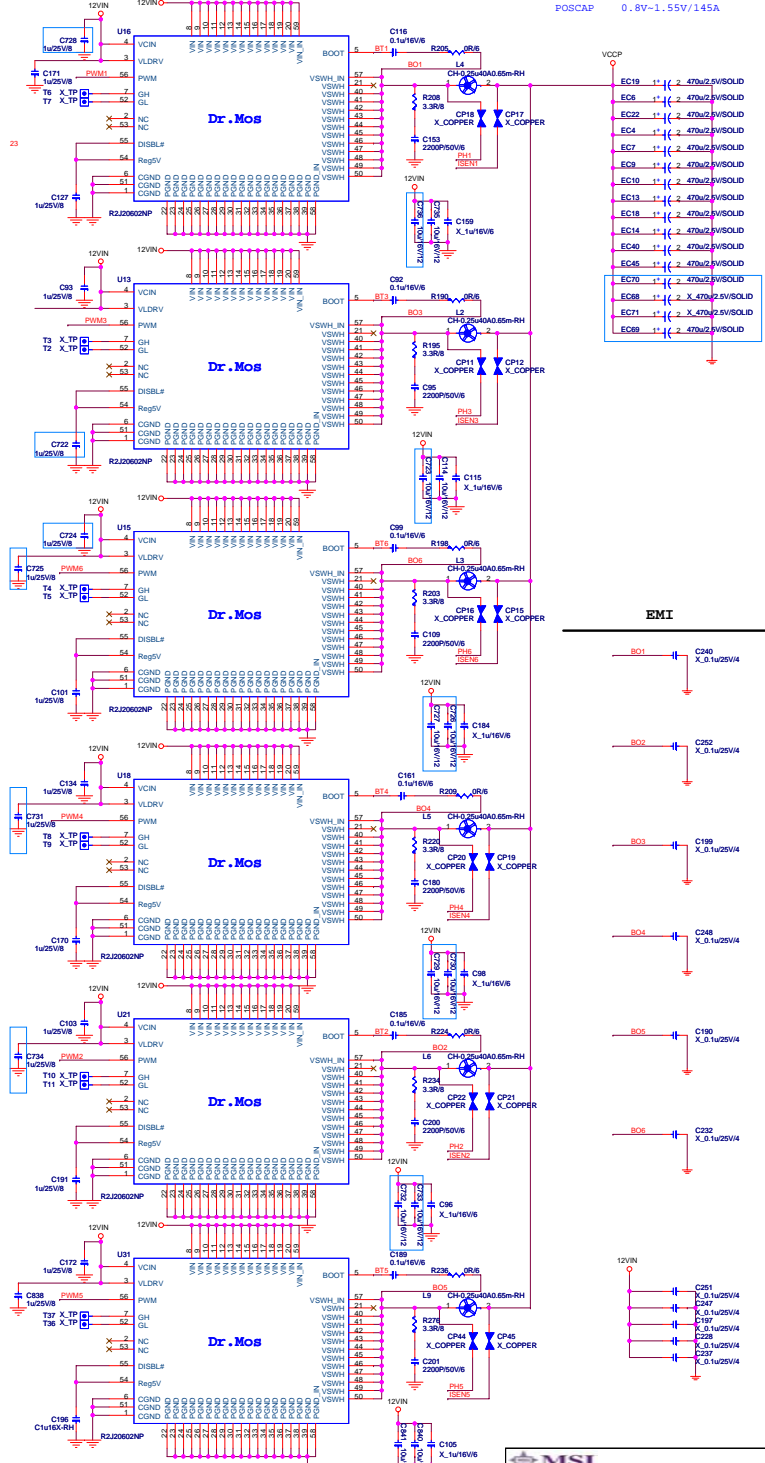
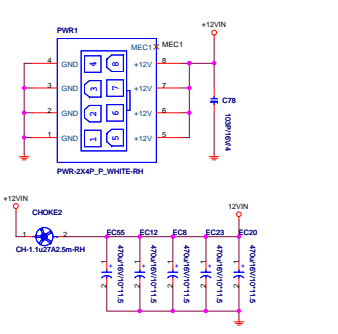
FRONT USB PORT 10,11



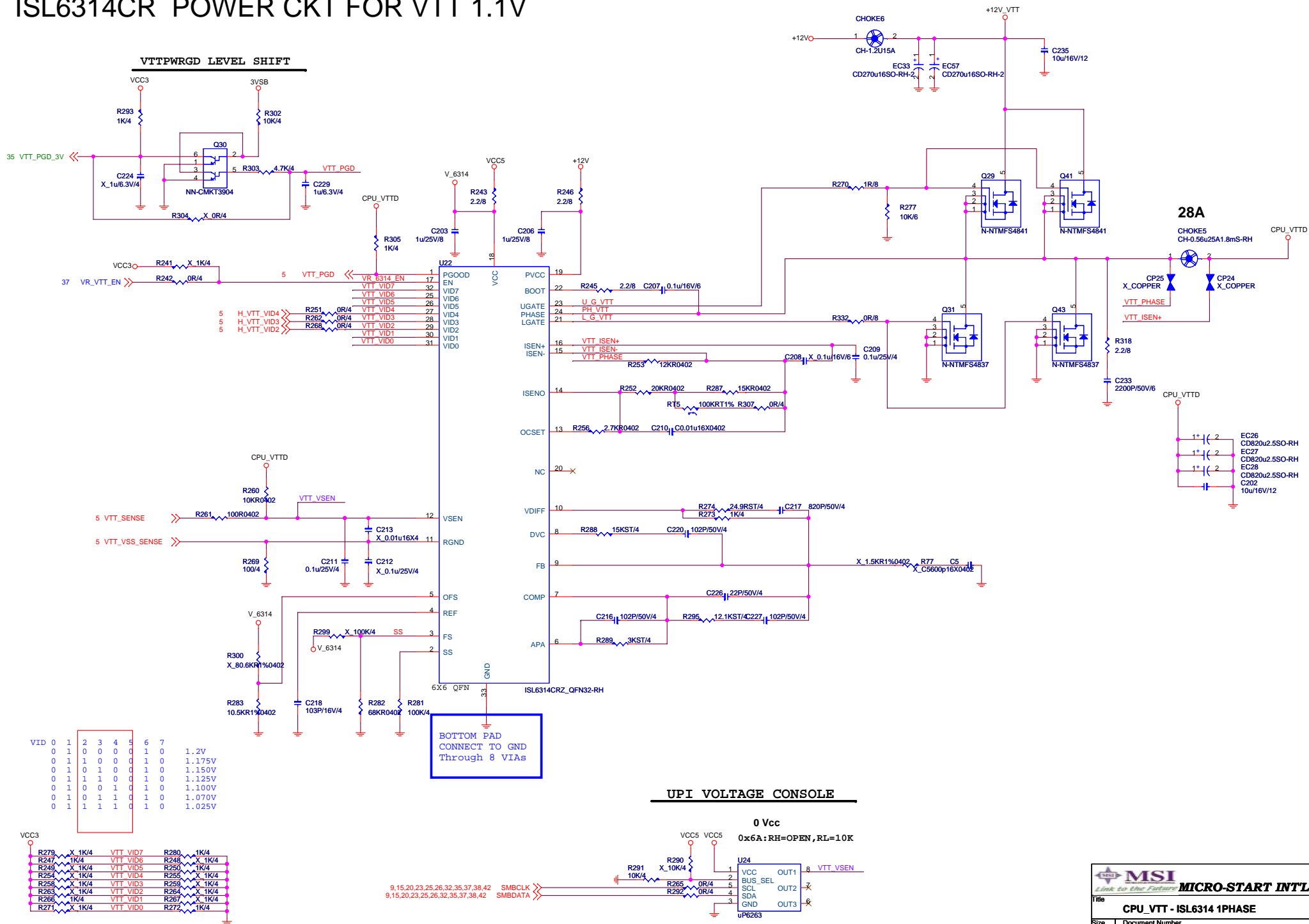
ISL6336CR VRD11.1 POWER CKT



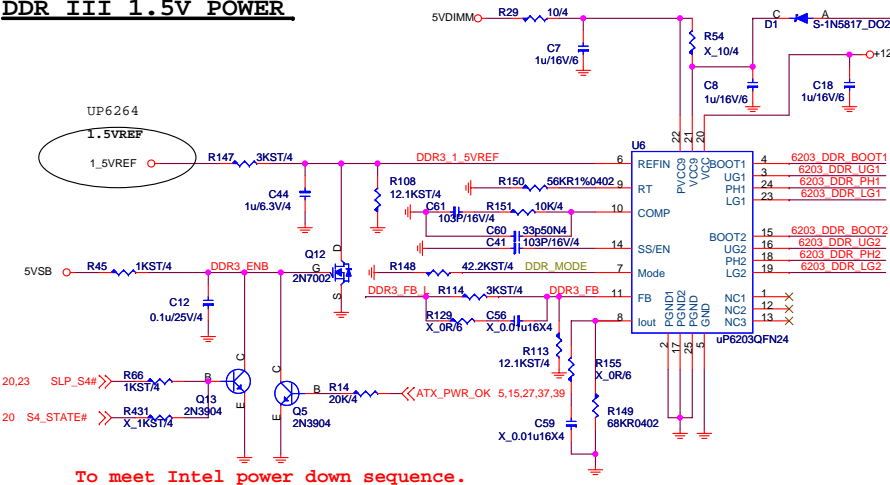
CPU +12VIN POWER CONN.



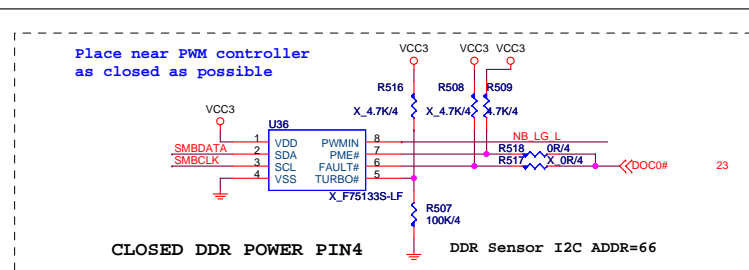
ISL6314CR POWER CKT FOR VTT 1.1V



DDR III 1.5V POWER



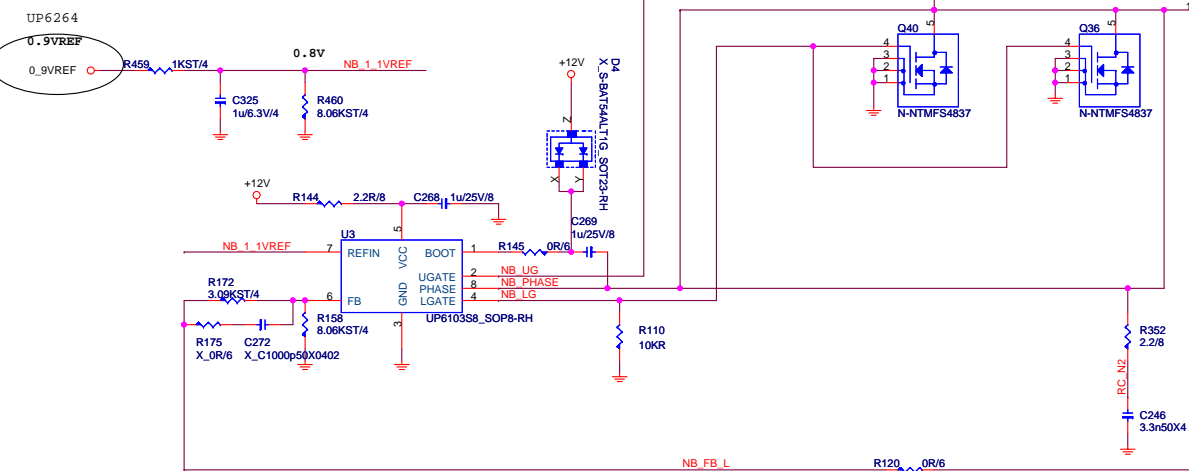
To meet Intel power down sequence.



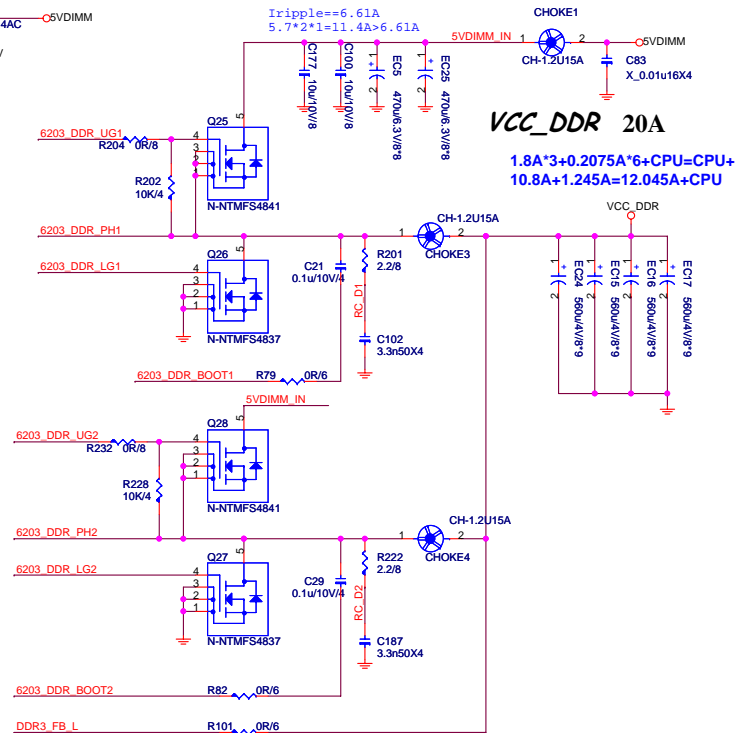
9,15,20,23,25,26,32,35,36,37,42 SMBDATA

9,15,20,23,25,26,32,35,36,37,42 SMBCLK

NB 1.1V POWER

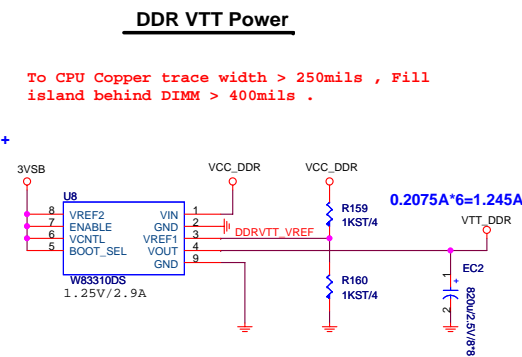


NB_FB_L R120 OR/6



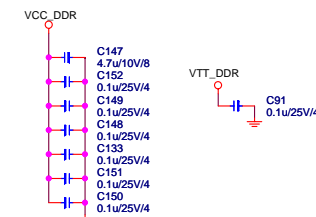
NB 1.1V

$$1.634A + 20.1A + 0.7A = 22.5A$$

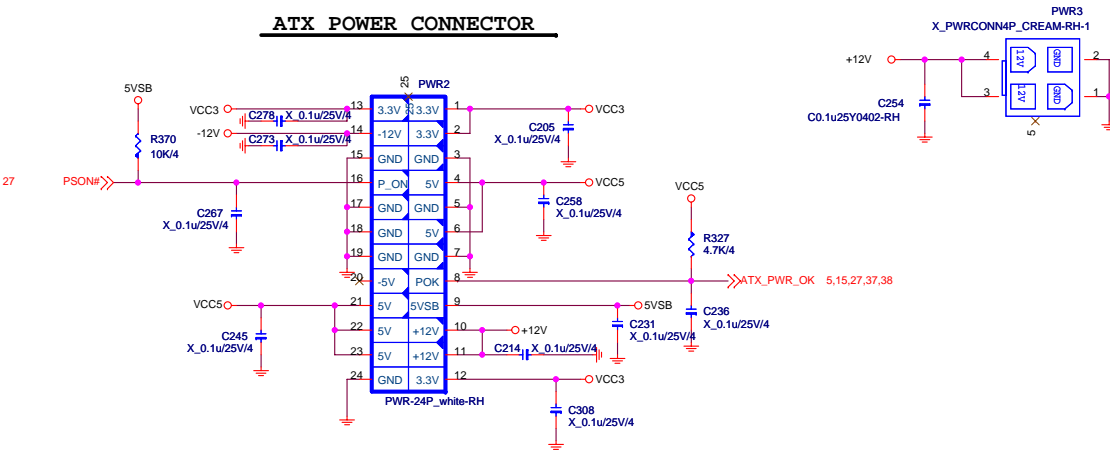


VR TO DIMM SOCKET

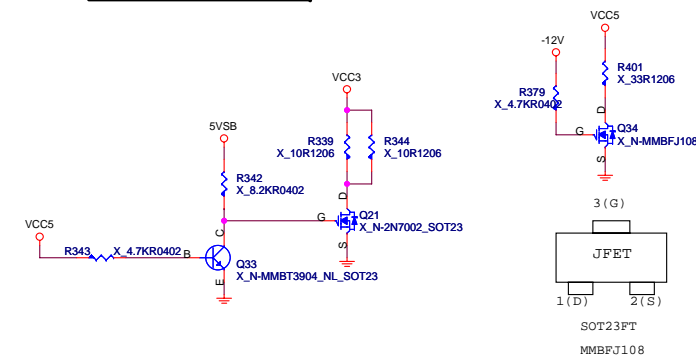
LDO TO DIMM SOCKET



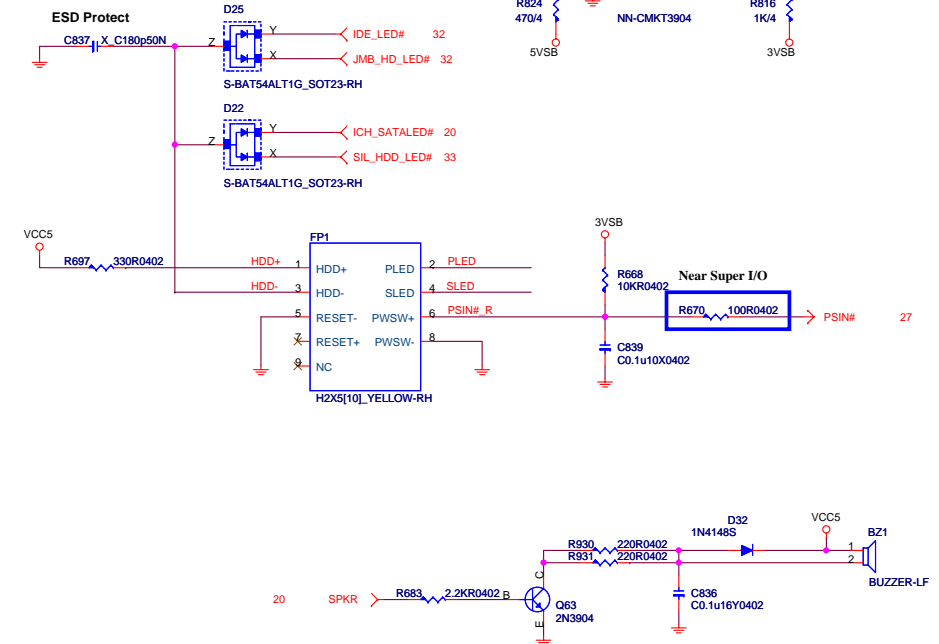
ATX POWER CONNECTOR



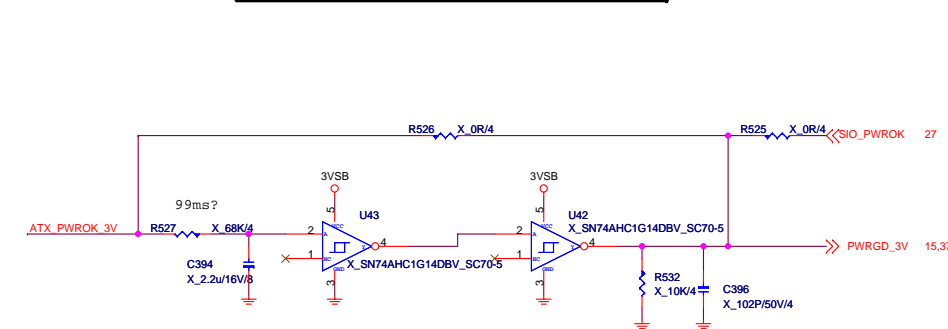
Minimum Load



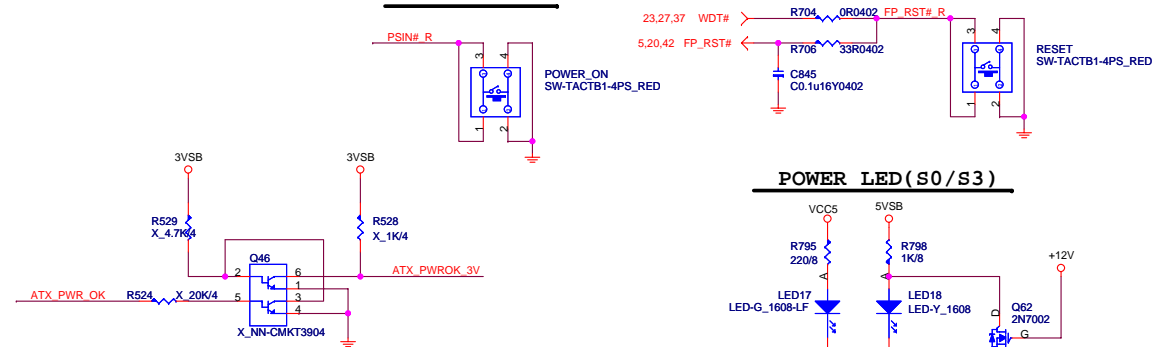
FRONT PANNEL



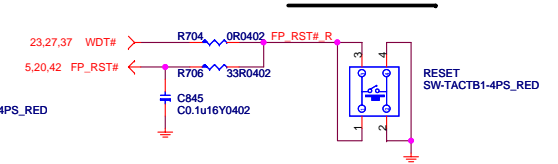
CHIPSET POWER GOOD CIRCUIT



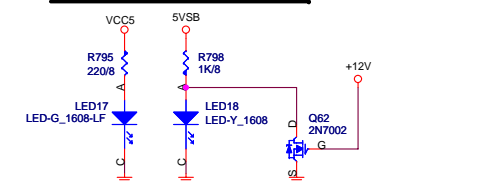
POWER ON BUTTON



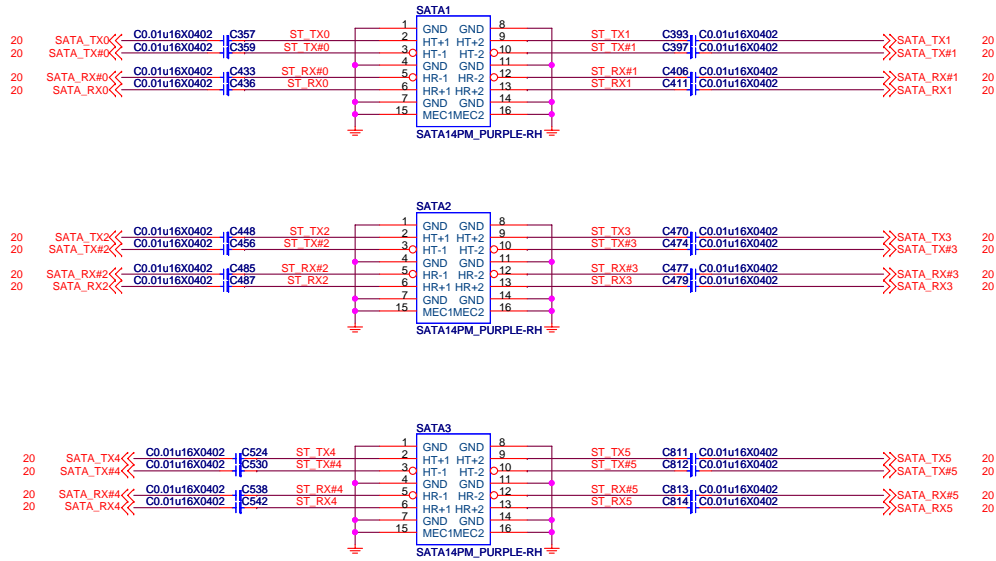
RESET BUTTON



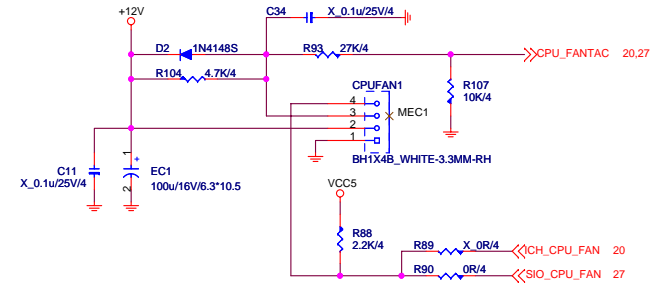
POWER LED (S0/S3)



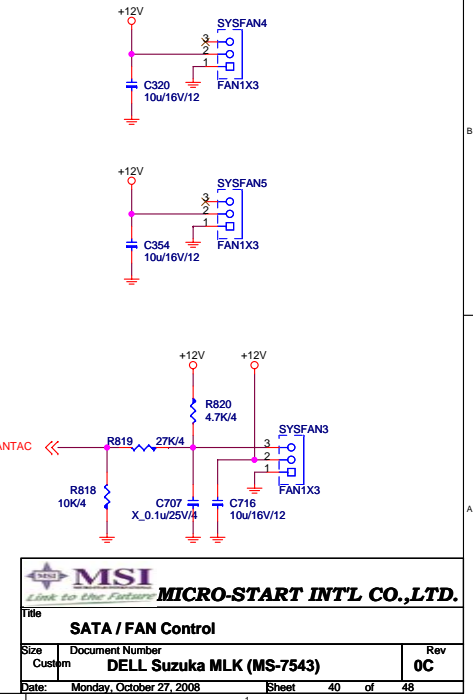
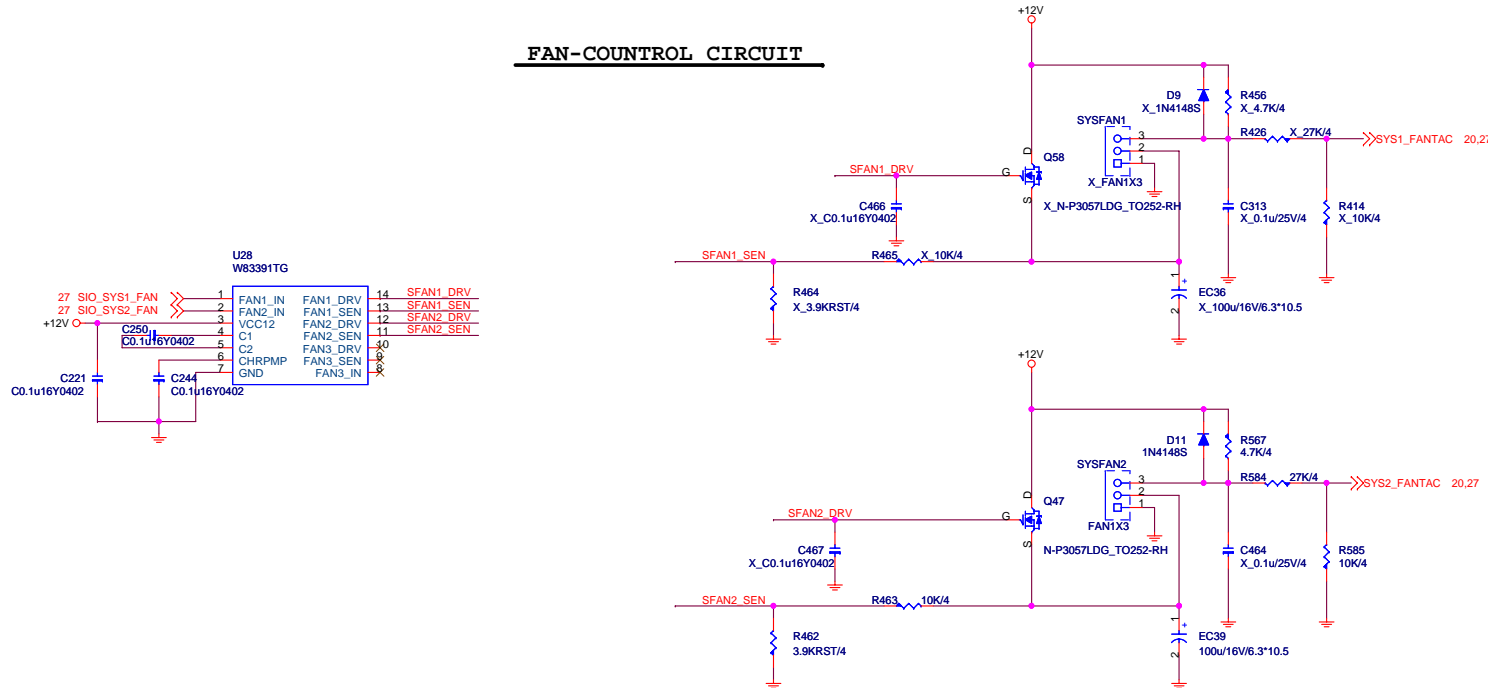
SATA-II Connector



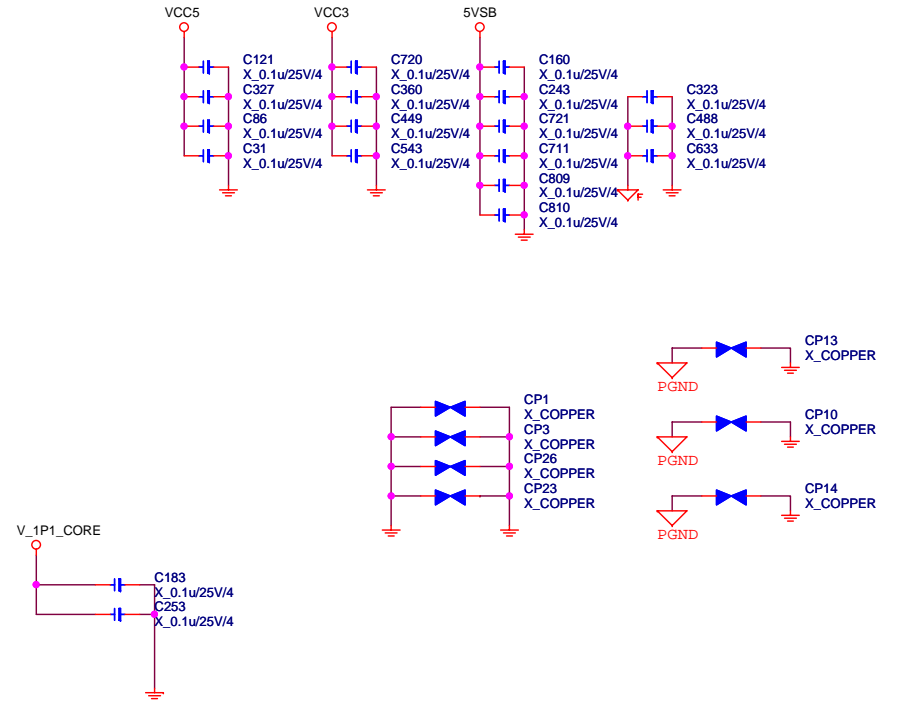
CPU FAN



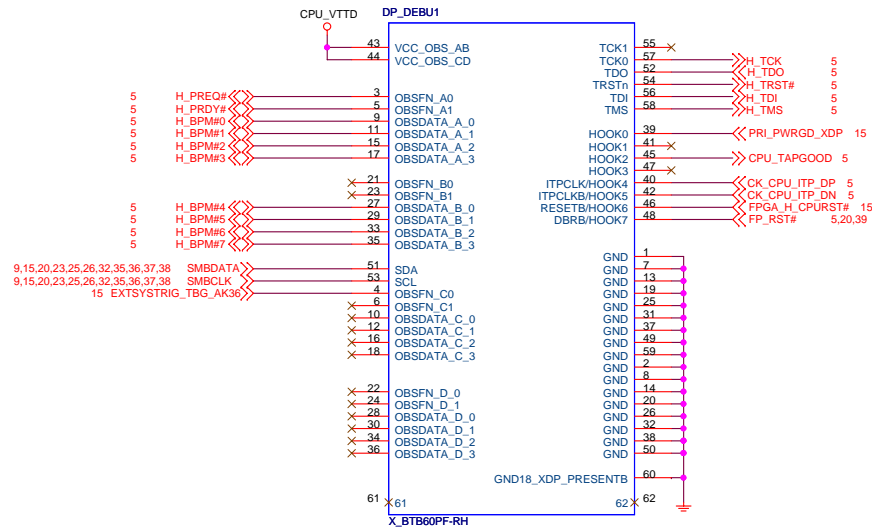
FAN-COUNTROL CIRCUIT



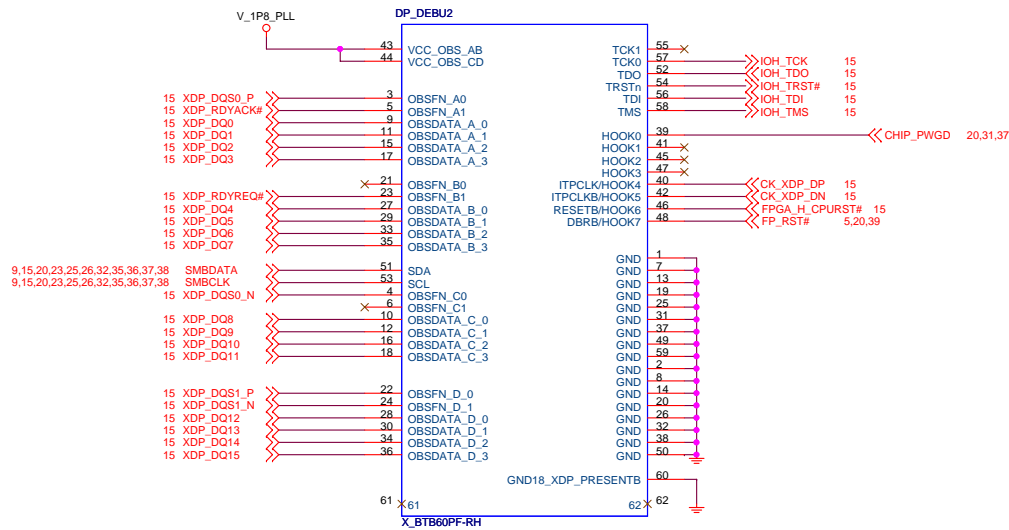
EMI CAP

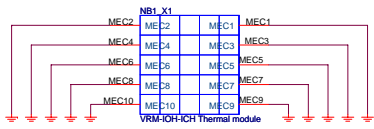


Reserve debug port 5020

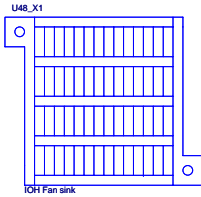


Reserve debug port 5020





PF0-0754310-BX2
PF0-0754310-TX3



BAT-BCR2032P-RH



E21-0000580

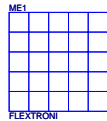
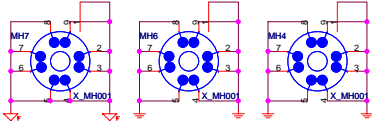
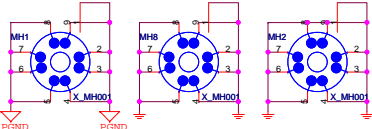
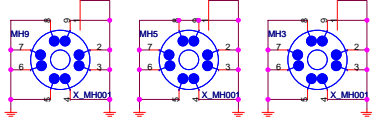
Optical Fiducial Marks-120



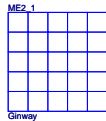
Optical Fiducial Marks-100



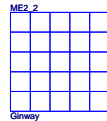
Mounting Holes



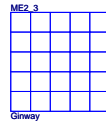
FLEXTRON



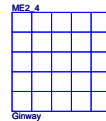
Ginway



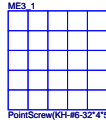
Ginway



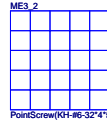
Ginway



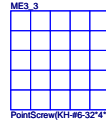
Ginway



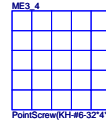
PointScrew(KH-#6-32*4*5 ZNW)



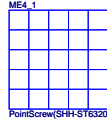
PointScrew(KH-#6-32*4*5 ZNW)



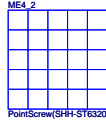
PointScrew(KH-#6-32*4*5 ZNW)



PointScrew(KH-#6-32*4*5 ZNW)



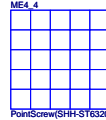
PointScrew(SHH-ST6320635ZNW-W)



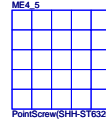
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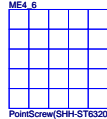
PointScrew(SHH-ST6320635ZNW-W)



PointScrew(SHH-ST6320635ZNW-W)



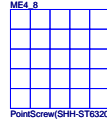
PointScrew(SHH-ST6320635ZNW-W)



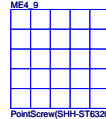
PointScrew(SHH-ST6320635ZNW-W)



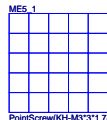
PointScrew(SHH-ST6320635ZNW-W)



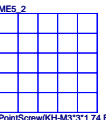
PointScrew(SHH-ST6320635ZNW-W)



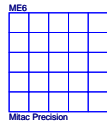
PointScrew(SHH-ST6320635ZNW-W)



PointScrew(KH-M3*3*1.74 BZ)



PointScrew(KH-M3*3*1.74 BZ)



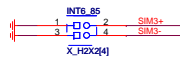
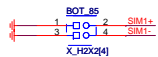
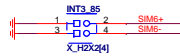
Mitac Precision

Simulation

4/8 95 ohm

5/5 85 ohm

5/7 85 ohm



Manual Parts

Size	Document Number	Rev
Custom	DELL Suzuka MLK (MS-7543)	0C
Date:	Monday, October 27, 2008	Sheet 43 of 48